

# 연구 분야 소개

한양대학교 ERICA 전자공학부

김종석



한양대학교  
HANYANG UNIVERSITY

# 이력 및 대표연구



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www.SIDLAB.net

총 40회 이상 반도체 IC Chip 개발



다양한 전자회로 시스템 개발



## 이력사항

- 2023 - 현재 : 조교수, 한양대 ERICA 전자공학부
- 2022 - 2023 : 조교수, 가천대 전자공학부
- 2018 - 2022 : 책임연구원, SK Hynix Flash 설계팀
- 2012 - 2019 : 박사과정, 한양대 전자컴퓨터통신공학과  
(학위논문: High-Reliability Gate Driver and Small-Area High-Resolution Data Driver for Flexible Active-Matrix Displays)

## 대표 연구실적

- **[Display Circuit]** IEEE ISSCC 2025 (반도체 올림픽), IEEE JSSC 2025 (under review)  
\*세계 최초 6285 PPI급 OLED-on-silicon display용 source driver IC 개발
- **[Display Circuit]** VLSI Symp 2026 (세계 최고 권위 회로 학회)  
\*세계 최소면적, 최고속도, 최고 균일도 source driver IC 개발
- **[Memory circuit]** IEEE ISSCC 2022 (반도체 올림픽)  
\*세계 최고 효율 최저 면적 flash memory 전원관리회로 개발
- **[Biomedical Circuit]** IEEE ESSERC 2025, IEEE TBioCAS 2025 (under review)  
\*세계 최초 비침습적 시간적 간섭 자극술 (Temporal Interference Stimulation) 회로 개발
- **[Biomedical Circuit]** Nat. Electron. 2021 (IF=33.25)  
\*세계 최초, 인간의 촉각인식 과정을 최대한 모사한 인공촉각 시스템 개발 (촉각 센서, 센서 readout 회로, 신경자극 회로)
- **[Sensor Circuit]** SID 2025  
\*세계 최초, Bottom-Emission OLED 디스플레이용 Touch Sensor 개발
- **[Sensor Circuit]** IEEE Sensors Journal 2023 (IF=4.3)  
\*세계 최초, active-matrix sensor 의 TFT on-resistance 영향을 제거한 회로 개발
- **[PMIC]** IEEE Trans. On Power Electronics 2022 (IF=5.97)  
\*세계 최초, 저잡음 고효율 특성을 동시에 갖는 PFM buck converter 개발

# Research Area

## World Best Next-Generation System IC Design 세계 최고 차세대 시스템 반도체 회로 설계

Display Circuit	Memory Circuit	AI Circuit	Sensor Circuit	Power Circuit	Biomedical Circuit
<p>AR/VR OLEDoS driving &amp; pixel circuit</p> <p>Micro-LED display Pixel &amp; driving circuit</p> <p>Compensation circuits for OLED &amp; Micro LED displays</p>	<p>Driving &amp; readout circuit for NAND flash memory</p> <p>Built-in-self-test (BIST) circuit for memory system</p> <p>High-efficiency charge pump &amp; regulator for NAND flash memory</p>	<p>Compute-in-memory circuit using TFT</p> <p>Calibration circuits for AI system</p> <p>Analog &amp; Digital TFT circuits for TFT CIM</p>	<p>Sensor circuit for Physical AI</p> <p>Touch &amp; Stylus sensor readout circuit</p> <p>Sensor uniformity enhancement circuit</p> <p>Readout circuits for R/L/C sensors</p>	<p>IoT PMIC</p> <p>GaN Driver</p> <p>Automotive PMIC</p> <p>Flash Memory PMIC</p> <p>Ultra-low-voltage LDO</p>	<p>Neural tactile sensing system</p> <p>Non-invasive brain stimulation circuit</p> <p>Neural stimulator</p> <p>Tumor treatment circuit</p>
<p>IEEE ISSCC 2025</p> <p>VLSI Symp. 2026</p> <p>IEEE TCAS-I 2026</p> <p>IEEE JSSC 2021</p>	<p>IEEE ISSCC 2022</p>	<p>IEEE TED 2018, 2017</p> <p>JJAP 2013, 2012</p>	<p>SID 2025</p> <p>Nature Elec. 2021</p> <p>IEEE Sensors 2025</p>	<p>IEEE TPE 2022</p> <p>AICSP 2016</p>	<p>IEEE ASSCC 2025</p> <p>Nature Elec. 2021</p>





# 연구분야

**디스플레이 회로**  
AR/VR OLED-on-Silicon (OLEDoS) LED-on-silicon (LEDoS) 회로



**OLEDoS 컬럼 구동회로**

**OLEDoS 화소회로**  
(4k X 4k, 6300 ppi, 3000 nit)

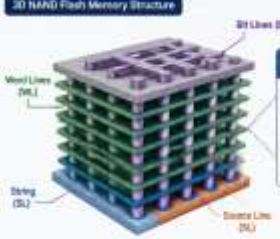


스캔 구동회로 (120 Hz frame rate)

에미션 구동회로 (120 Hz frame rate)

\*Substrate: Silicon

**메모리 회로**  
DRAM / Flash memory 용 Analog 회로설계



**3D NAND Flash Memory Structure**

Vertical Lines (VL), Bit Lines (BL), Memory Cell (Vertical Channel), Control Gate, Floating Gate, Tunnel Oxide, Channel, Blocking Gate, Source Line (SL), String (SL).

3D NAND Flash requires high-voltage operation: (Program / Erase / Read) across multiple stacked layers.

**High Voltage Requirements in 3D NAND**

Operation	Typical Voltage
Program (PROM)	15 V ~ 20 V
Erase (ERASE)	-10 V ~ -12 V
Read (R)	2 V ~ 8 V

High voltage is essential to control the charge in deeply stacked cells. Charge Pump Circuit provides these voltages.

**High-Efficiency Charge Pump Circuit**  
(Used in 3D NAND Flash Memory System)

N Stages (Multi-Stage Charge Pump)

STAGE 1, STAGE 2, STAGE N

Input Voltage:  $V_{in} (0.2V)$

High Voltage Output:  $V_{out} (15V-20V)$

Stage & Clock Controller

CLK (Input)

Charge Generator, Non-overlapping Clocks, Control Logic

**Key Role in 3D NAND Flash Memory**

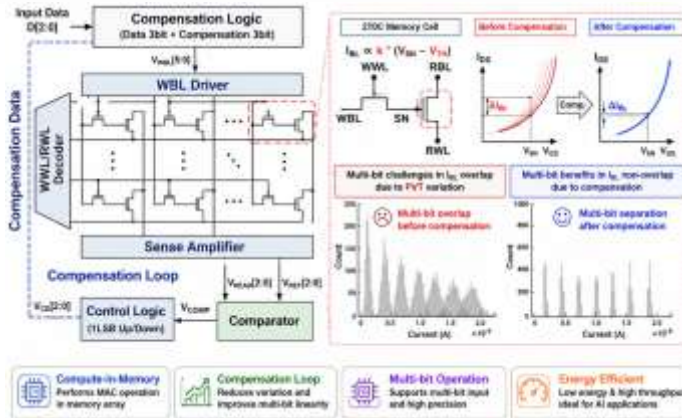
- Supports Deep Vertical Stacking: Generates high voltages for multi-layer cell operation.
- Enables Program / Erase: Provides precise high-voltage pulses for reliable cell control.
- Improves Reliability: Stable high-voltage generation ensures data retention and endurance.
- High Efficiency & Low Power: Optimized multi-stage design reduces power in memory systems.



# 연구분야

## AI 회로

### Compute-in-Memory (CIM) 회로

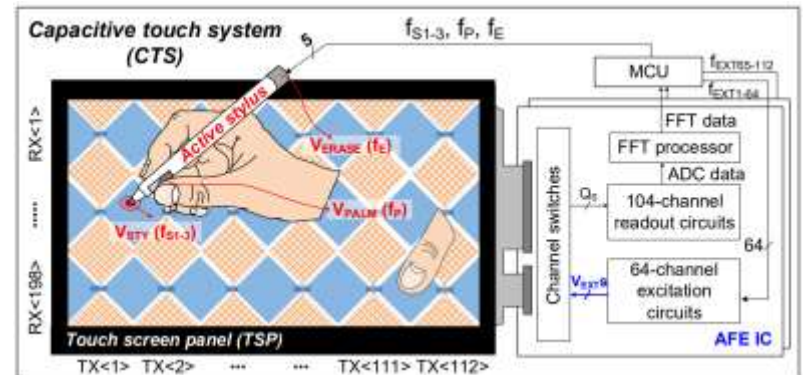


협력기관



## 센서회로

### OLED in-cell touch & stylus sensor ROIC



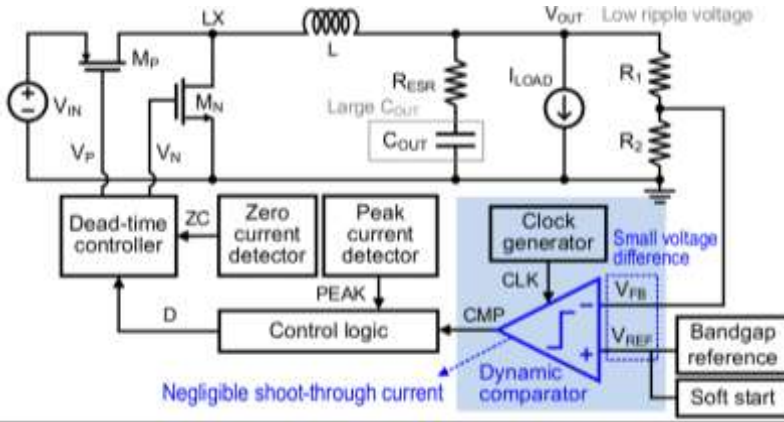
협력기관



# 연구분야

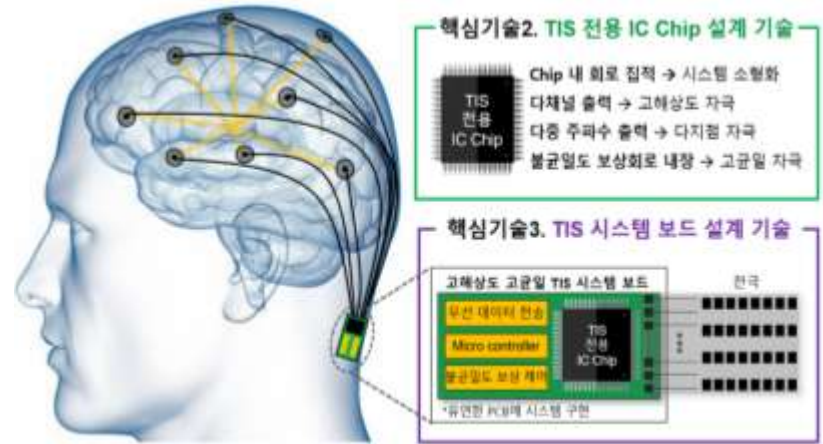
## Power 회로

차량용 PMIC, Mobile용 PMIC, LDO, Charge pump



## 바이오메디컬 회로

비침습적 뇌자극 회로 개발



협력기관



협력기관










# System IC Design Lab (SIDLAB) -연구원 & 연구시설-

## 연구원 현황

대학원생	2026년 5월
 박사과정 & 석박통합과정	4
 석사과정	7
 학부연구생	5

## 설계/실험 장비 구축 현황

	수량	사양 / 비고
 Oscilloscope	5 EA	2.5GHz, 4CH
 Power supply	12 EA	3CH, 0.1mV/0.1mA Res.
 Function generator	5 EA	100 MHz
 Digital I/O	2 EA	32 Ch, 200 MHz
 Digital multimeter	2 EA	6.5 digit
 Workstation	6 EA	-
 EDA tool	완비	Synopsys, Cadence, Siemens 등

## 실험실 및 실험장비 구축 완료



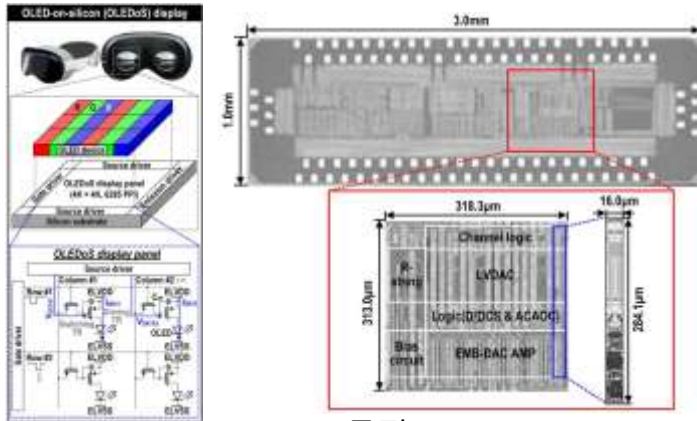
## 실험 환경



# 최근 연구 성과

IEEE ISSCC 2025 발표  
(세계 최고권위 회로 학회)

고해상도, 저면적, 고균일  
OLED-on-Silicon (OLEDoS) 구동 IC chip 개발

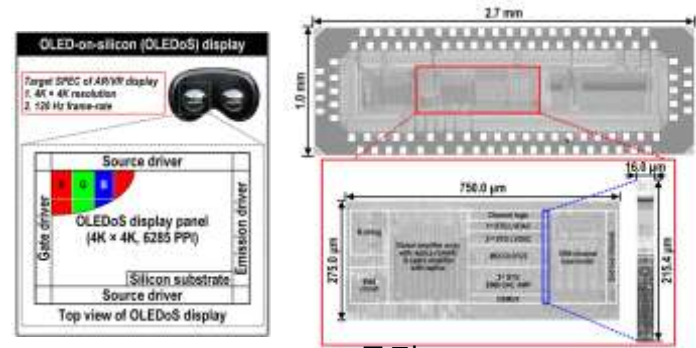


공정: TSMC 65nm



IEEE VLSI. Symp 2026 발표  
(세계 최고권위 회로 학회)

고해상도, 저면적, 고균일  
OLED-on-Silicon (OLEDoS) 구동 IC chip 개발



공정: TSMC 65nm

중앙일보



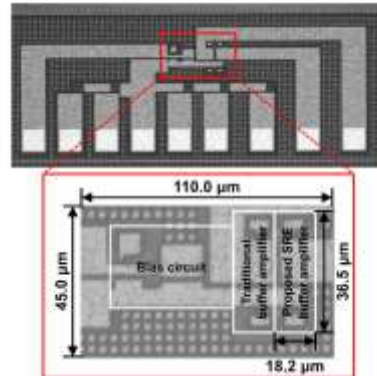
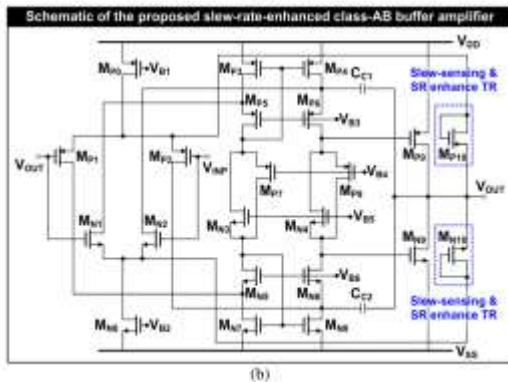
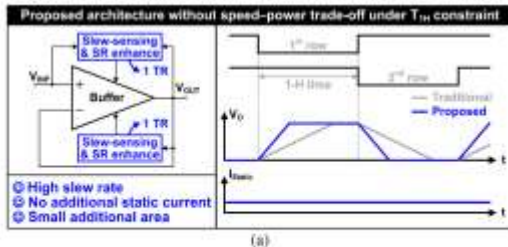
문화일보



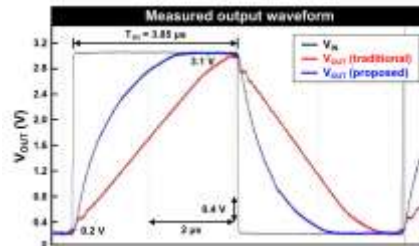
# 최근 연구 성과

IEEE TCAS-I 2026  
(Major 회로 저널)

전류 재사용 방식의  
저전력 고속 Amplifier 회로 개발

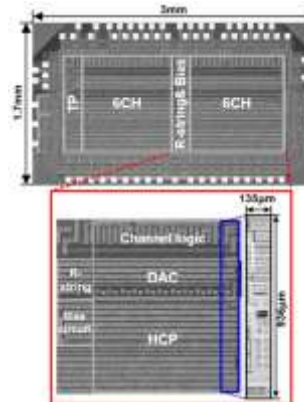
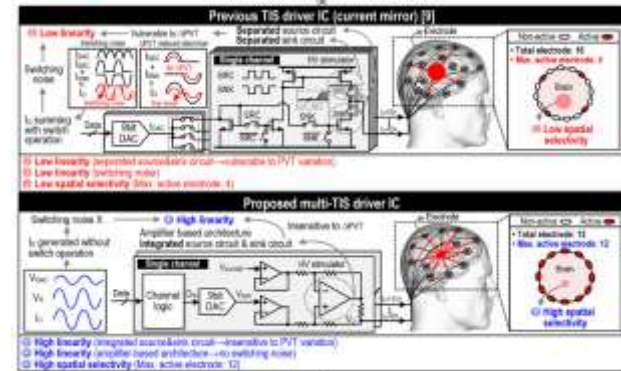


공정: TSMC 180nm BCD (40V)



IEEE ASSCC 2025 발표  
(Major 회로 학회)

세계 최초 비침습적 뇌자극  
multi-TIS driver IC chip 개발



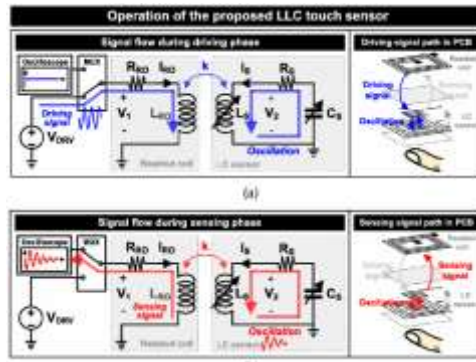
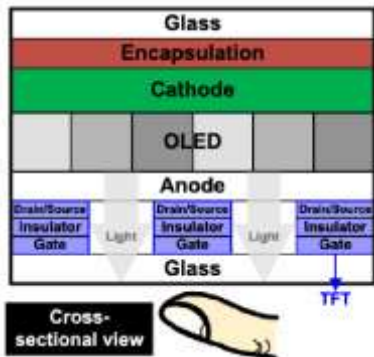
공정: TSMC 180nm BCD (40V)



# 최근 연구 성과

IEEE SID 2025 발표  
(세계 최고권위 디스플레이 학회)

세계 최초 Bottom-Emission Display용  
Inductor 기반 터치센서 및 전용회로 개발



# 최근 연구 성과

## 김종석 교수, 세계 최고 권위 반도체 학술대회 ISSCC TPC 위원으로 선 정돼

한양대학교 ERICA 전자공학부 김종석 교수가 반도체 집적화로 분야에서 세계 최고 권위를 자랑하는 IEEE International Solid-State Circuits Conference(ISSCC)의 기술 프로그램 위원회(Technical Program Committee, TPC) 위원으로 선정되었다.

한양대학교 ERICA 전자공학부 김종석 교수가 반도체 집적화로 분야에서 세계 최고 권위를 자랑하는 IEEE International Solid-State Circuits Conference(ISSCC)의 기술 프로그램 위원회(Technical Program Committee, TPC) 위원으로 선정되었다.

ISSCC는 1954년 시작된 이후 반도체 회로 분야의 최신 기술과 혁신이 가장 먼저 공개되는 글로벌 최고 권위 학술대회로, 반도체 회로 분야의 올림픽으로 불린다. 인텔, 삼성전자, TSMC 등 글로벌 선도 기업과 세계 유수 대학 연구진이 참여하며, 학계와 산업을 아우르는 기술 발전의 중심 속 역할을 수행하고 있다.

김종석 교수는 이번 TPC 위원 선정을 통해 제출 논문의 엄정한 심사, 우수 논문 선정, 기술 세션 및 플래너리 프로그램 기획 등 학계의 핵심 의사결정 과정에 참여하게 된다. ISSCC TPC 위원은 해당 분야에서 탁월한 연구 성과와 국제적 영향력을 인정받은 연구자들에게만 초청되는 자리로, 매우 제한된 인원만이 참여할 수 있는 최고 수준의 학술적 위상으로 평가된다.

김종석 교수는 SK hynix에서 NAND 플래시 메모리를 마닐라 회로 설계 등을 수행하며 산업계에서의 실무 경험을 쌓았으며, 이후 Nature Electronics, IEEE Journal of Solid-State Circuits, IEEE Transactions on Power Electronics 등 세계적 권위의 학술지에 연구 성과를 발표하여 국제적 연구 경쟁력을 입증해 왔다. 특히 한양대학교 ERICA 부임 이후에는 사스-코로나 바이러스 팬데믹 분야에서 세계 최고 수준의 연구 성과를 단기간 내 연속적으로 창출하며, ISSCC 2025, VLSI Symposium 2026, ASSCC 2025 등 최고 권위 국제 학술대회에서의 연속적인 성과를 바탕으로 이번 TPC 위원에 선정되었다. 이는 산업계 경험과 학문적 성과가 결합된 경쟁력을 바탕으로 이룬 결과로, 김종석 교수 개인의 연구 역량뿐만 아니라 우리 대학 신자립학 분야의 연구 경쟁력이 세계적 수준에 도달했음을 보여주는 중요한 성과로 평가된다.

향후 김종석 교수는 ISSCC TPC 위원으로서 글로벌 반도체 기술 트렌드를 선도하고, 자체 집적회로 기술의 방향성을 설정하는 데 핵심적인 역할을 수행할 것으로 기대된다.

### 최신뉴스

- 한양대, 2026 미래 예술융합 아카데미 신년 행사
- 한양대, 2026 융합영어인재교육 국제심포지엄
- 광고인 공 무는 한우 대학생활, 한스 학생 어워드
- 논리의 후손에 관심 있다면... 장학금과 해외 학
- "자위성-리더십 수확" 한양대 학생복지위원회

### 포토뉴스



### 연기 TOP10

- 1 한양대, '빅데이터융합' 기술적 계획... 글로벌 아
- 2 한양대, 2026 라제오스 : 한양 라인업 공개대회



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[연구분야: 디스플레이 회로]

# AR/VR 기기용 Micro Display 회로

# Publication: ISSCC 2025

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## Publication:

ISSCC 2025(반도체 올림픽), San Francisco, California, USA, Feb. 2025

## Title:

A 10b Source-Driver IC with All-Channel Automatic Offset Calibration and Slew-Rate-Enhanced Amplifier Achieving  $2273\mu\text{m}^2/\text{Channel}$  and 1.9mV DVO for 6285-PPI OLED-on-Silicon Displays



# Background

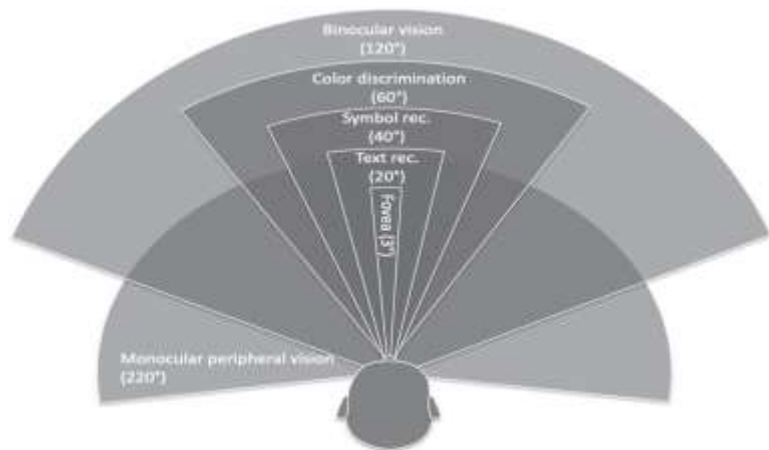
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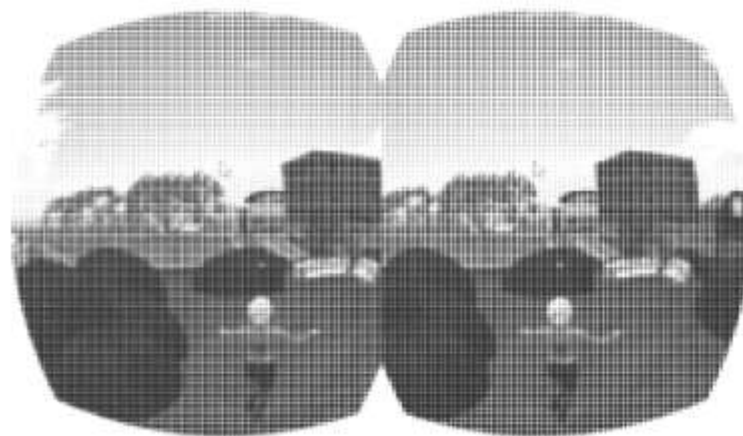
Image: Apple, Vision Pro

# Background -Resolution-

## Field of view (FoV)



## Pixel per degree (PPD)



Required specification	
Field of view (FoV)	Horizontal: 120°*, Vertical: 120°*
Pixel per degree (PPD)	60PPD*
<b>Resolution</b>	<b>7.2K × 7.2K</b> (120×60) × (120×60)

\*120° FoV and 60PPD are required for realistic vision.

# Background -Frame Rate-

Low frame rate



Dizziness, blurred vision

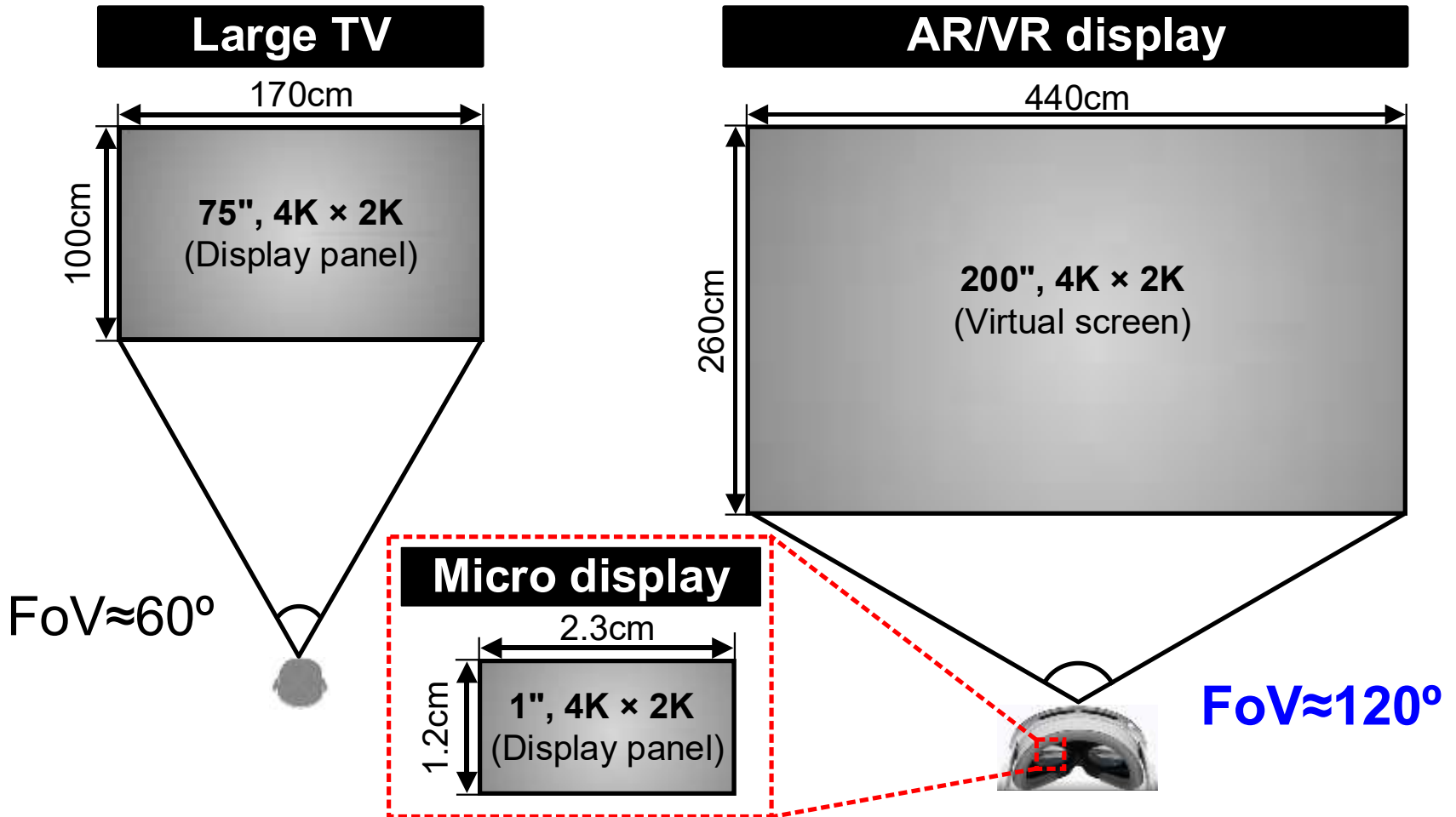
High frame rate



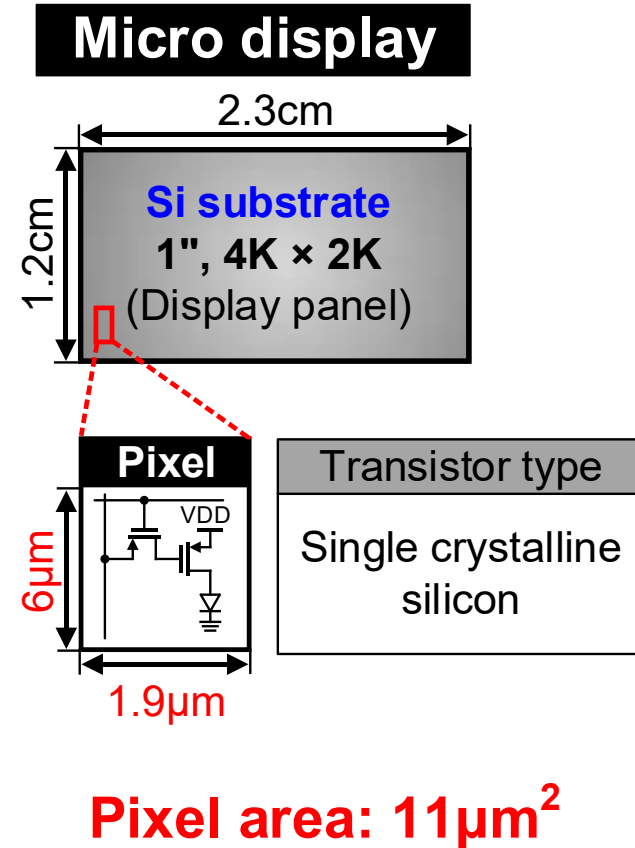
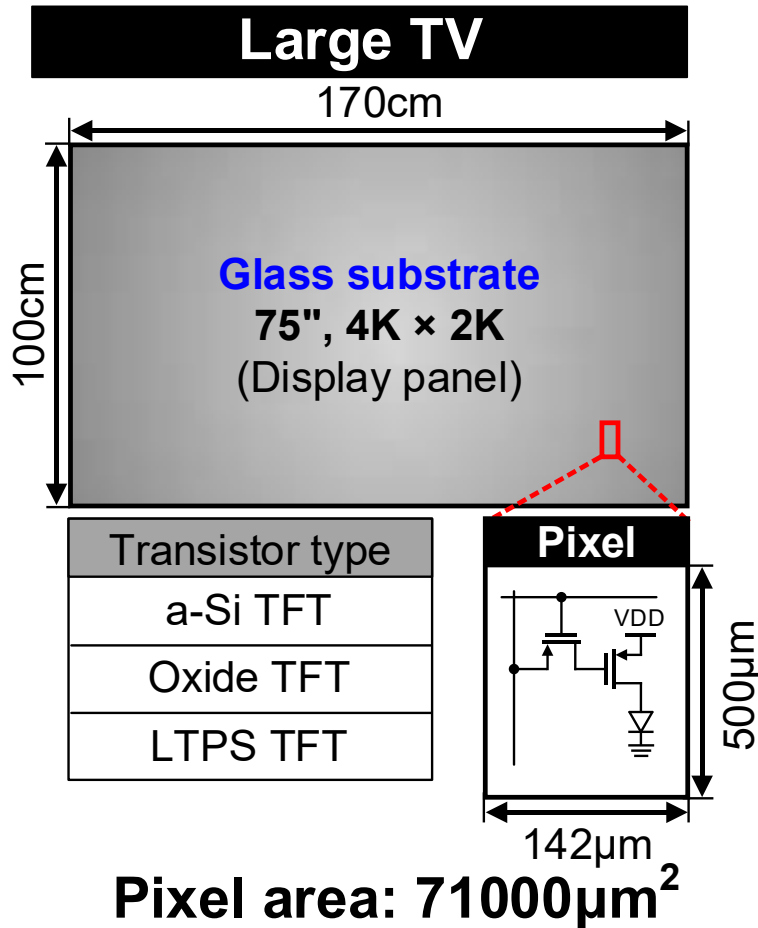
No dizziness, clear vision

- Frame rate of at least 120Hz is required.

# Background -Micro Display for AR/VR Device-

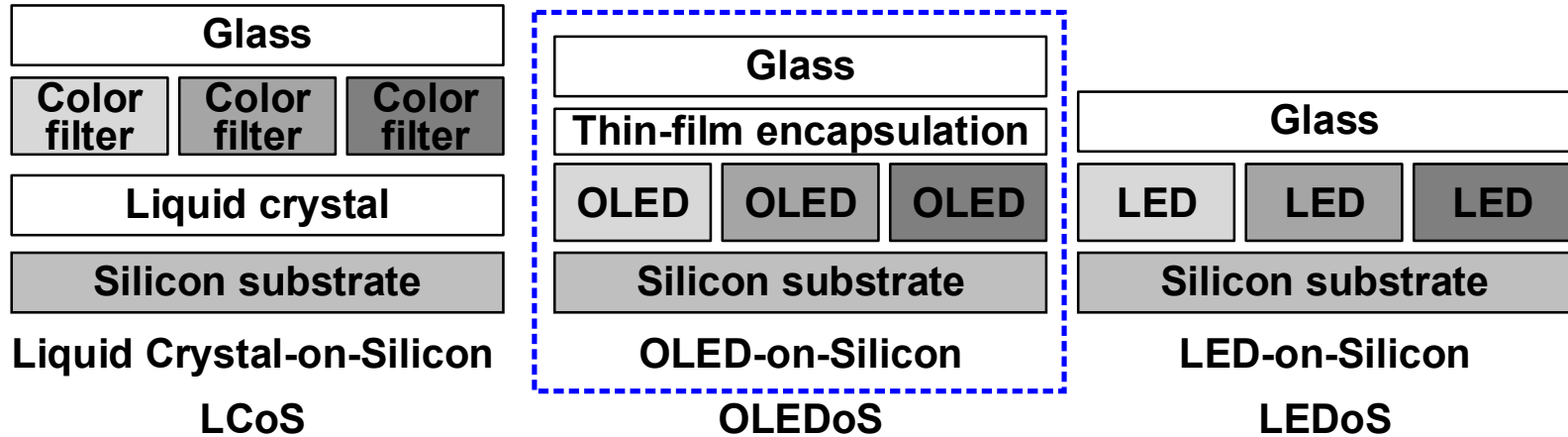







# Background -Pixel Size-



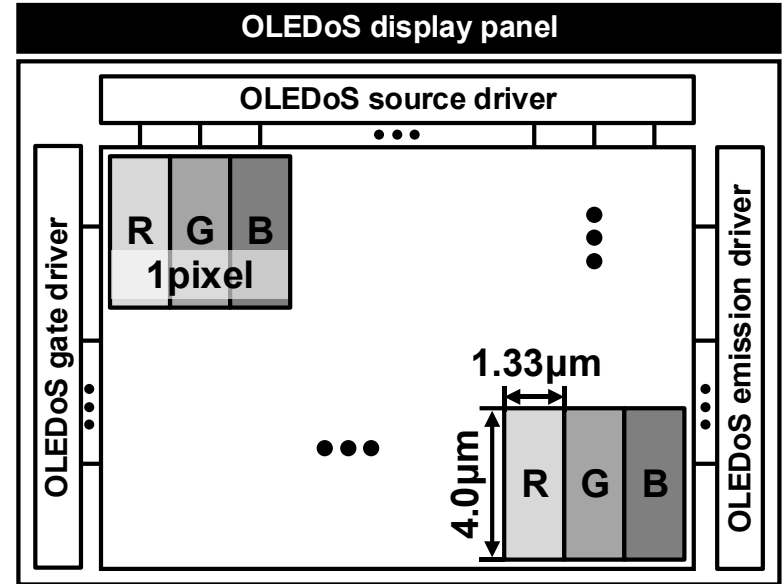
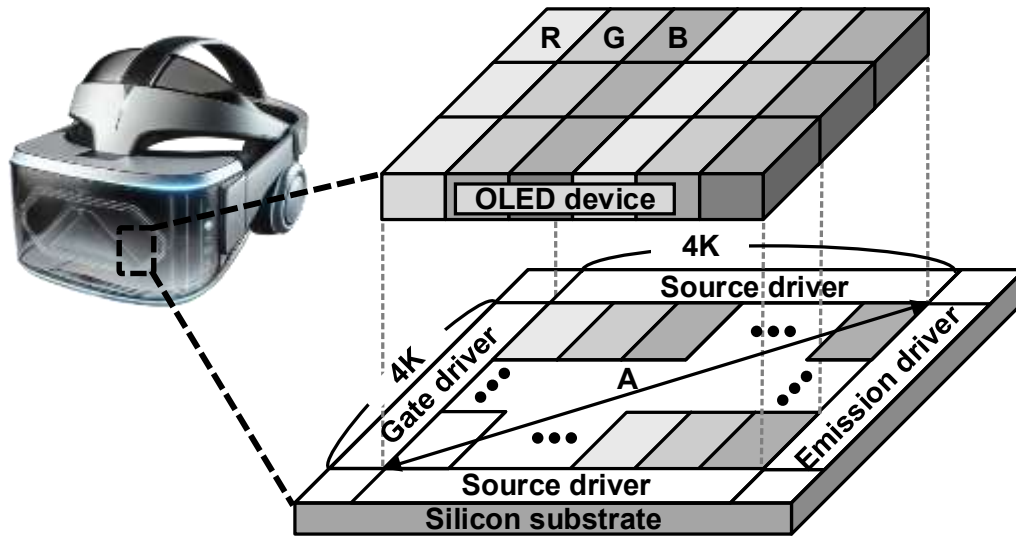
- Small pixel area is required → silicon substrate & CMOS process

# Background -AR/VR Device Application-



Application	AR glass		VR headset			This work
Manufacturer	Rokid	Xreal	Apple	Meta	Pico	-
Product name	Joy 2	One Pro	Vision Pro	Quest 3	Pico 4 ultra	-
Release year	2024	2025	2024	2023	2024	2025
Technology	OLEDoS	OLEDoS	OLEDoS	LCOS	LCOS	OLEDoS
Resolution(per eye)	1920×1080	1920×1080	3660×3200	2064×2208	2160×2160	4000×4000
Diagonal size(inch)	-	0.55	1.41	2.48	2.56	0.9
Pixel per inch(PPI)	-	-	3386	1218	1200	6285
Frame rate(Hz)	120	120	100	120	90	120
Image						-

# Background -Architecture of OLEDoS Display-

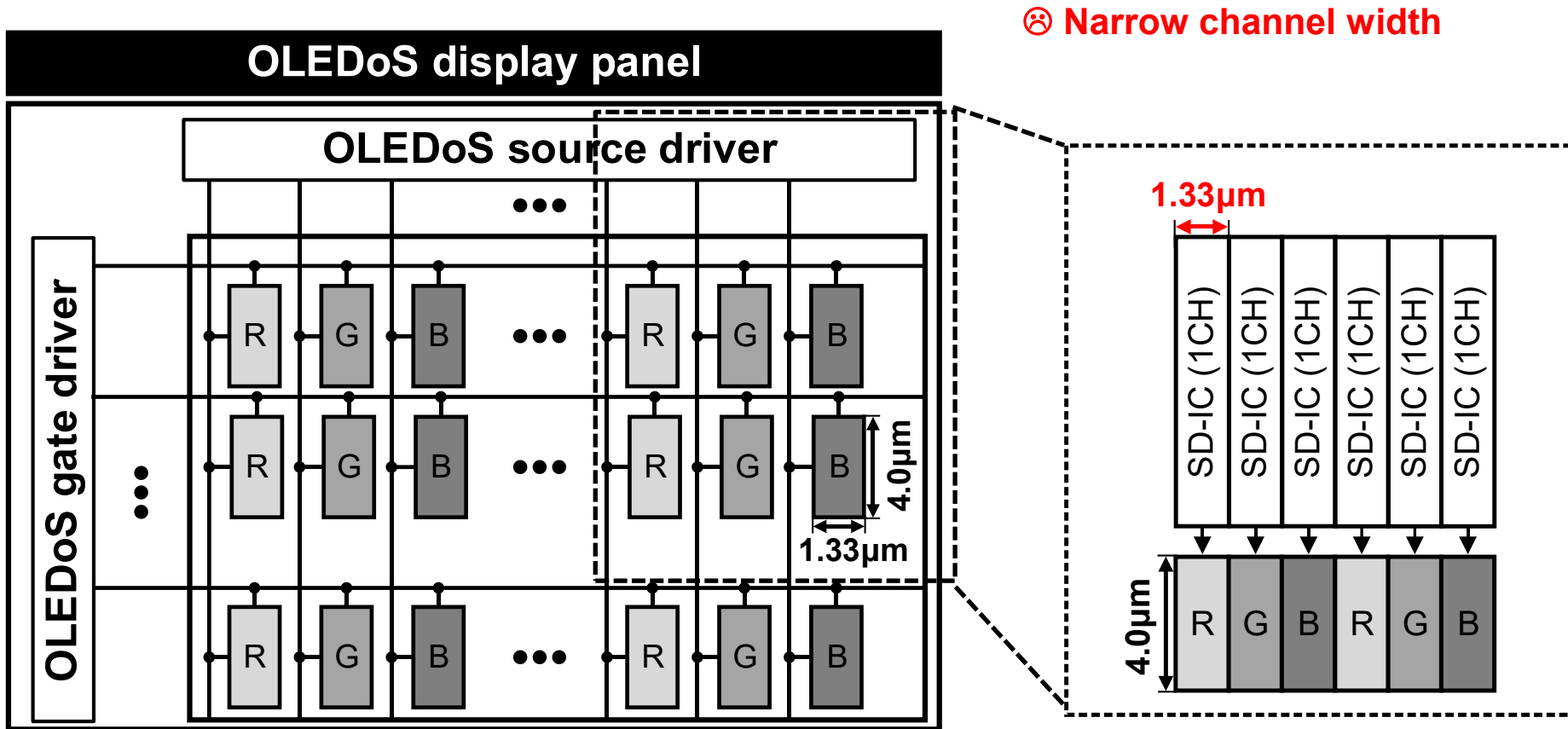


\*1 pixel = 3 sub pixels (R,G,B)

## Design specifications for OLEDoS display panel

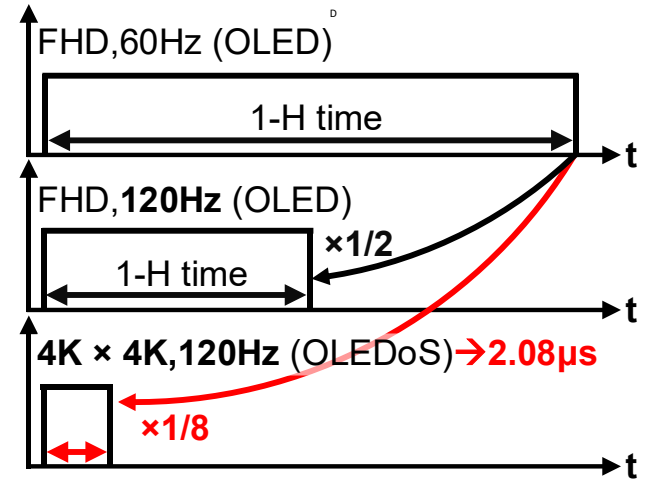
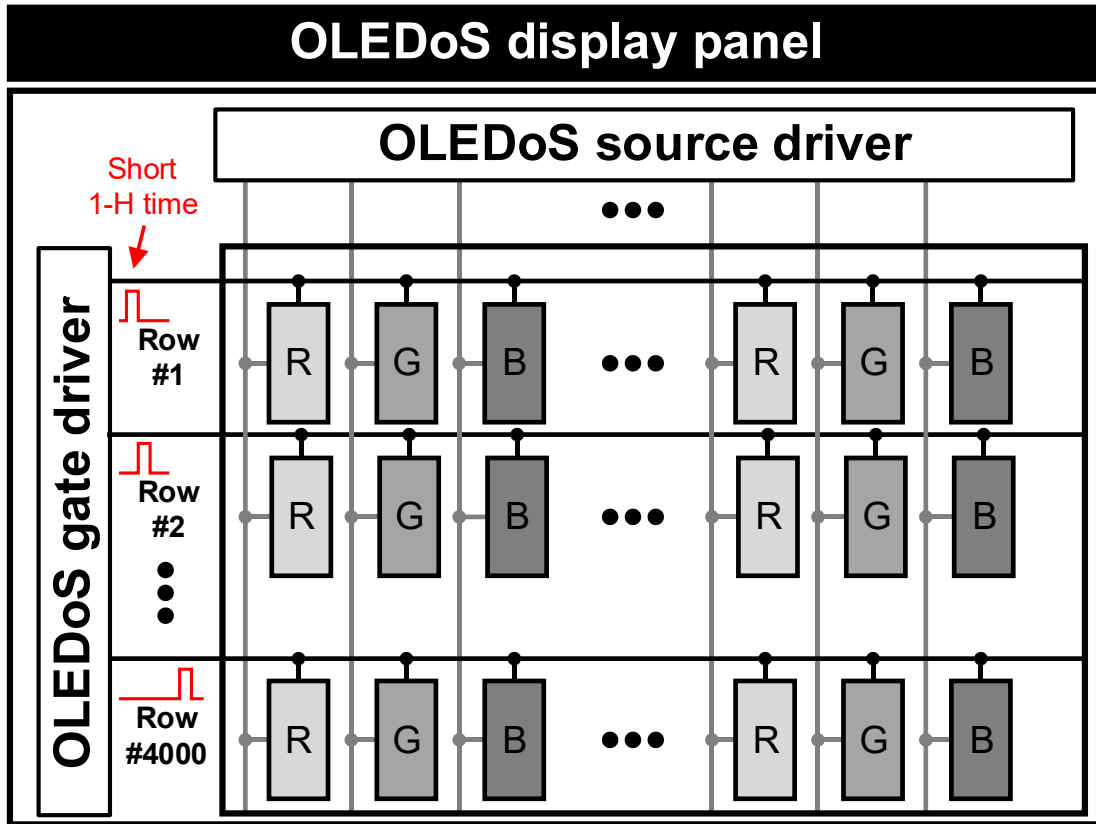
Diagonal size (A)	0.9"	$PPI = (C \times \sqrt{2}) / A$	6285PPI
Resolution (C)	4K × 4K	Pixel pitch = 1inch/PPI	4.0µm

# Background -OLEDoS Challenge 1: Narrow Channel Width-



- Requirement: **Small-area source driver IC (SD-IC)**

# Background -OLEDoS Challenge 2: Short 1-H Time-

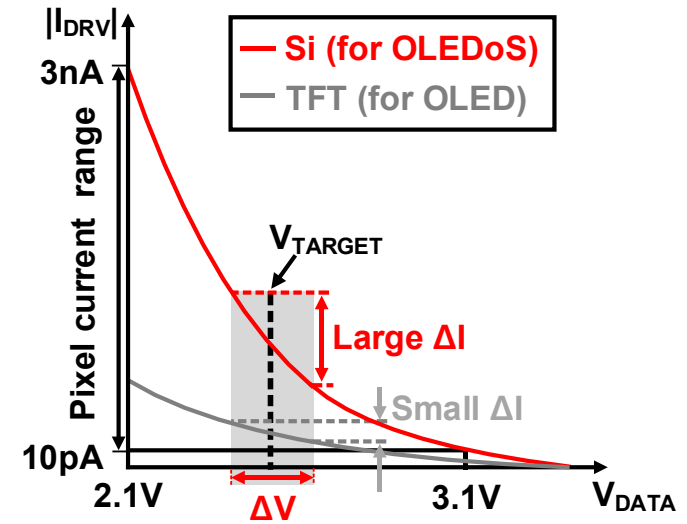
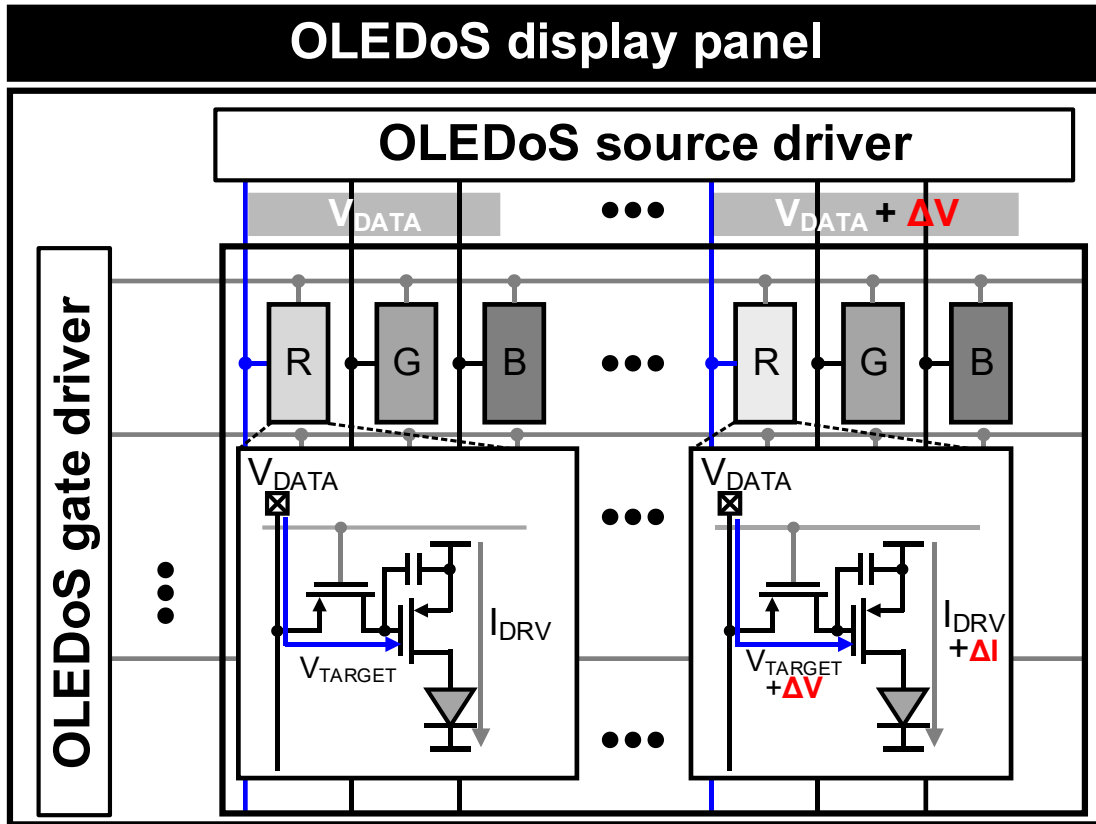


⊗ Short 1-H time

$$1\text{-H} = \frac{1}{\text{Number of row line} \times \text{frame rate}}$$

- Requirement: **Fast SD-IC**

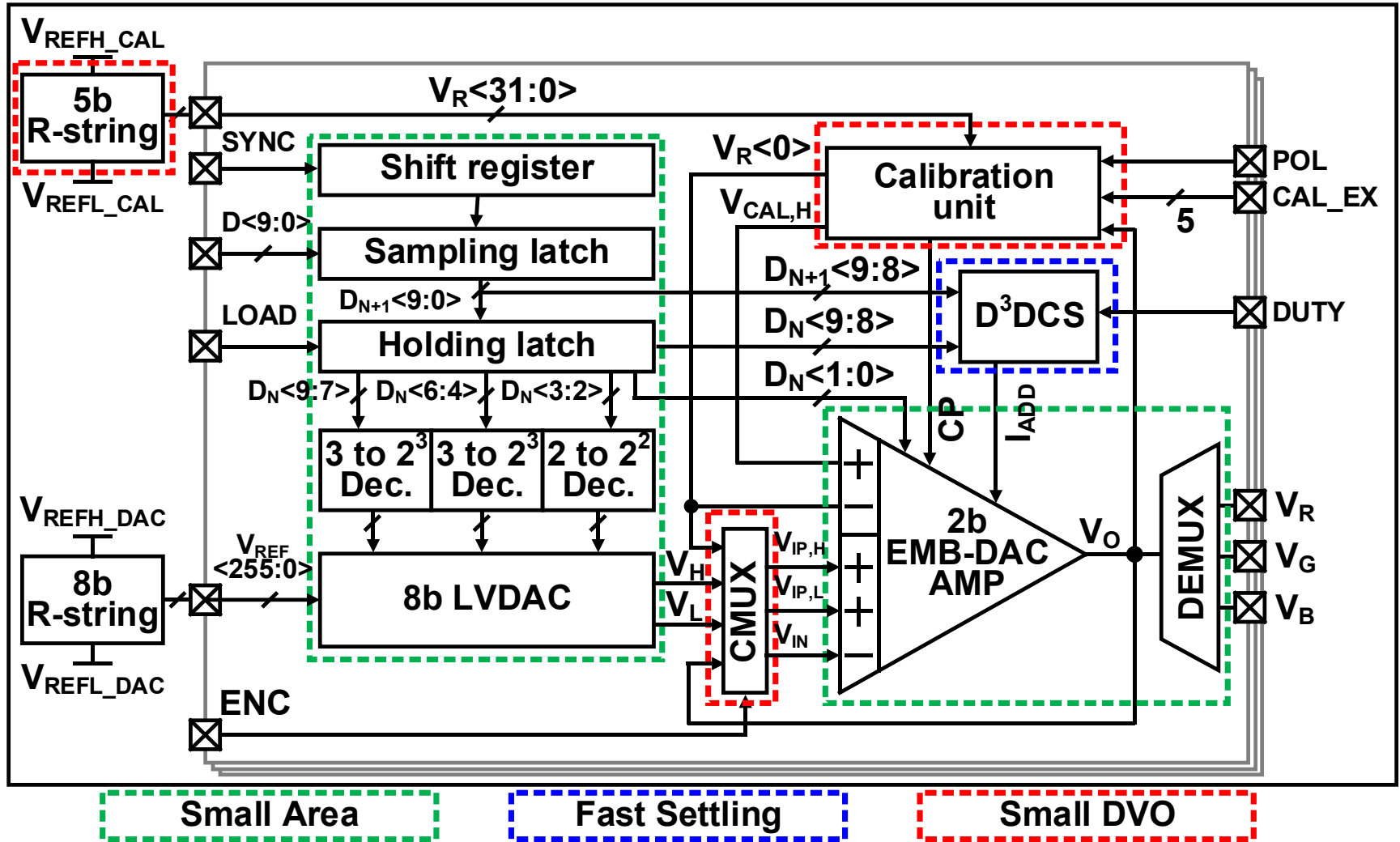
# Background -OLEDoS Challenge 3: Voltage Deviation-



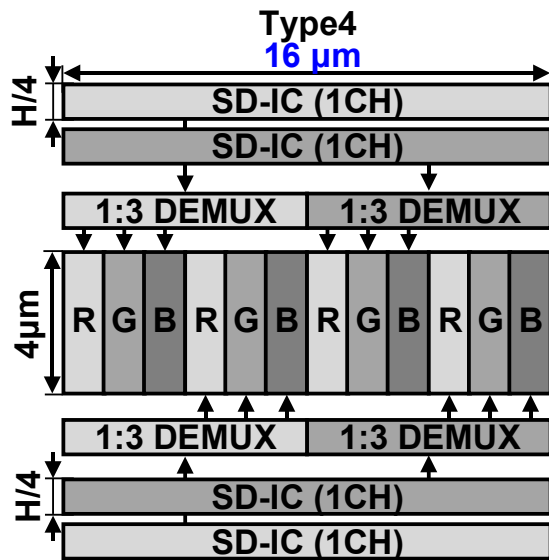
⊗ Voltage variation of SD-IC  
→ pixel current variation

- Requirement: **Small deviation of voltage output (DVO) SD-IC**

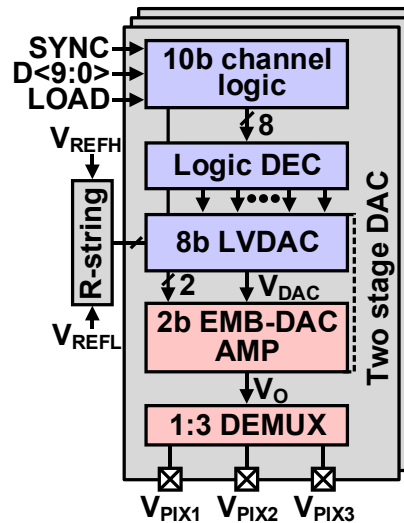
# Proposed OLEDoS SD-IC -Architecture of SD-IC-



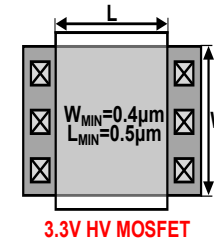
# Small-Area SD-IC -Methods to Achieve Small Area-



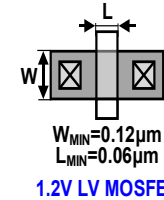
## Proposed 10b SD-IC



Large size  
HV MOSFET

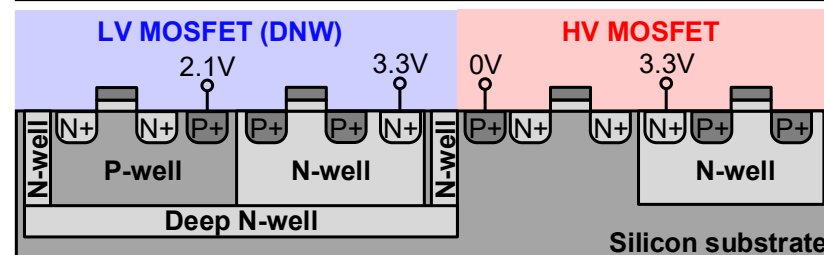


Small size  
LV MOSFET



LV MOSFET HV MOSFET

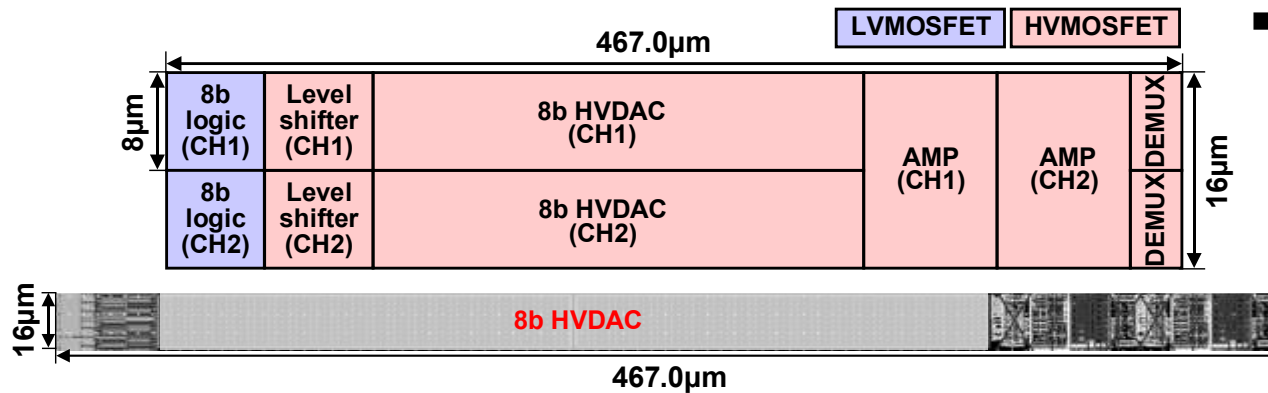
## LV MOSFET (DNW) and HV MOSFET structure



- 1:3 DEMUX → small area
- LV MOSFET → small area
- Deep N-well → small area
- 2b EMB-DAC AMP & logic decoder → # of DAC switches ↓ → small area

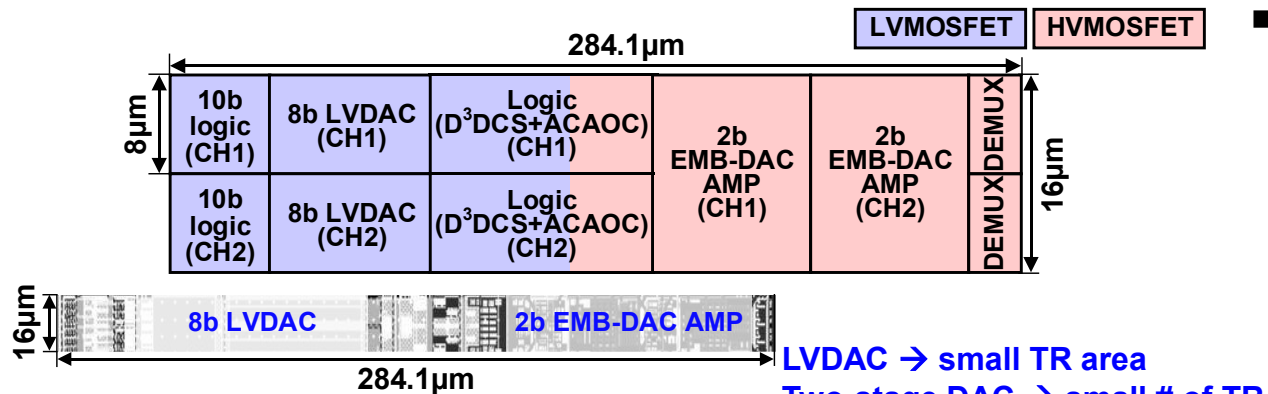
# Small-Area SD-IC -Area Comparison-

## Conventional 8-bit source driver (2 channels)



- **Large area**  
→ conventional 8b HVDAC

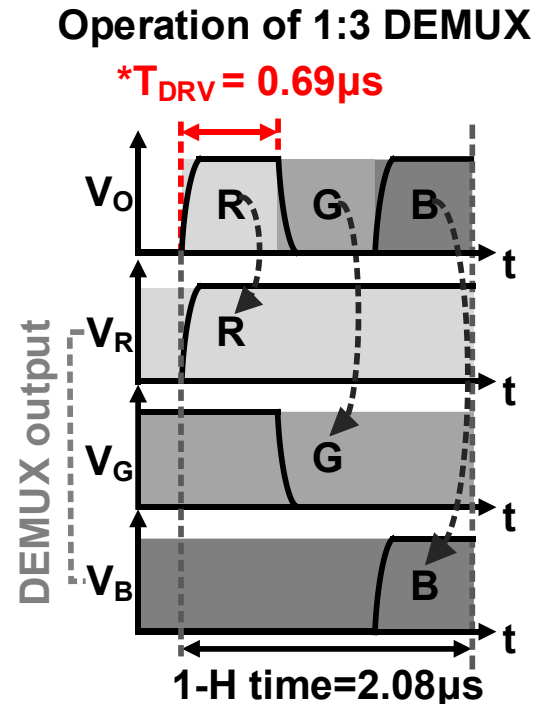
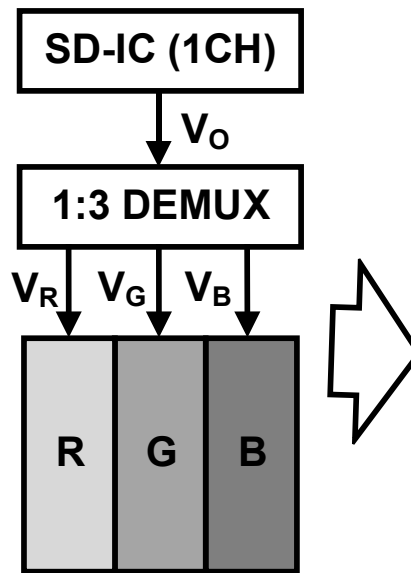
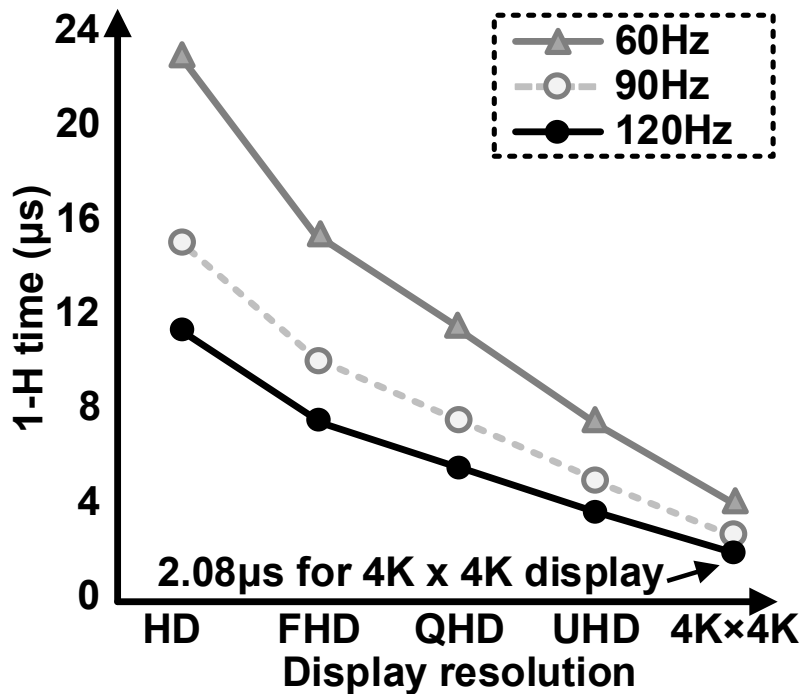
## Proposed 10-bit source driver (2 channels)



- **Small area** proposed 10b DAC  
→ 8b LVDAC + 2b EMB-DAC AMP

LVDAC → small TR area  
Two-stage DAC → small # of TR

# Fast SD-IC -Short Settling Time-

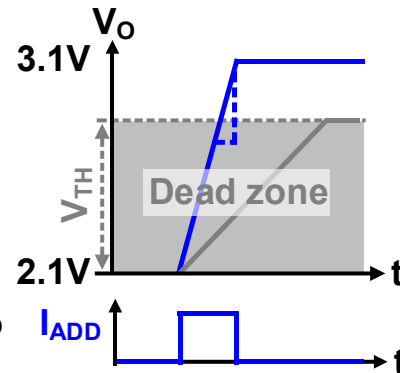
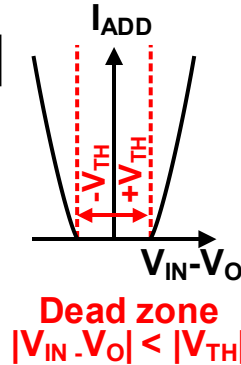
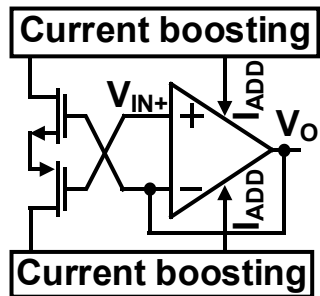


$$*Driving\ time(T_{DRV}) = \frac{1}{4K \times 120\ Hz \times 3} = 0.69\mu s$$

- For 4K x 4K resolution, 120 Hz frame rate, and 1:3 DEMUX  
 → setting time ≤ **0.69µs**

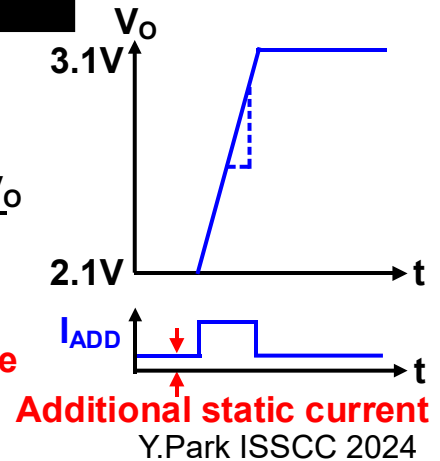
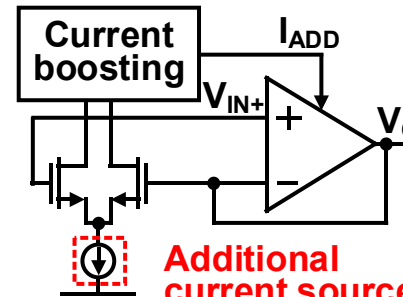
# Fast SD-IC -Limitations of Prior Works-

## Prior work ①



G.-G. Kang SOVC 2021

## Prior work ②



Y.Park ISSCC 2024

### ⊗ Deadzone

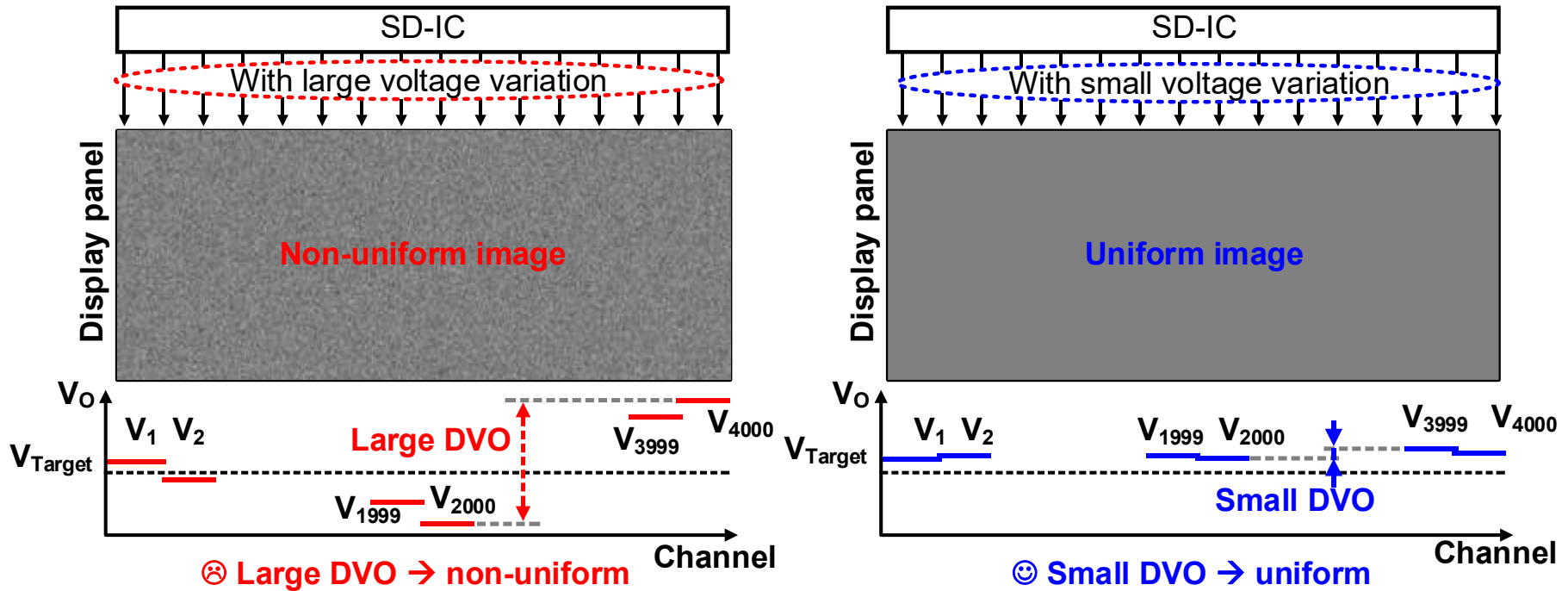
- To turn on boosting circuit, the IN/OUT difference should be larger than  $V_{TH}$ .
  - Small difference
    - Current boosting is **not activated**.

### ⊗ Additional static current

- To compare the IN/OUT difference, a comparator is used.
  - Additional static current
    - **Increased static power**

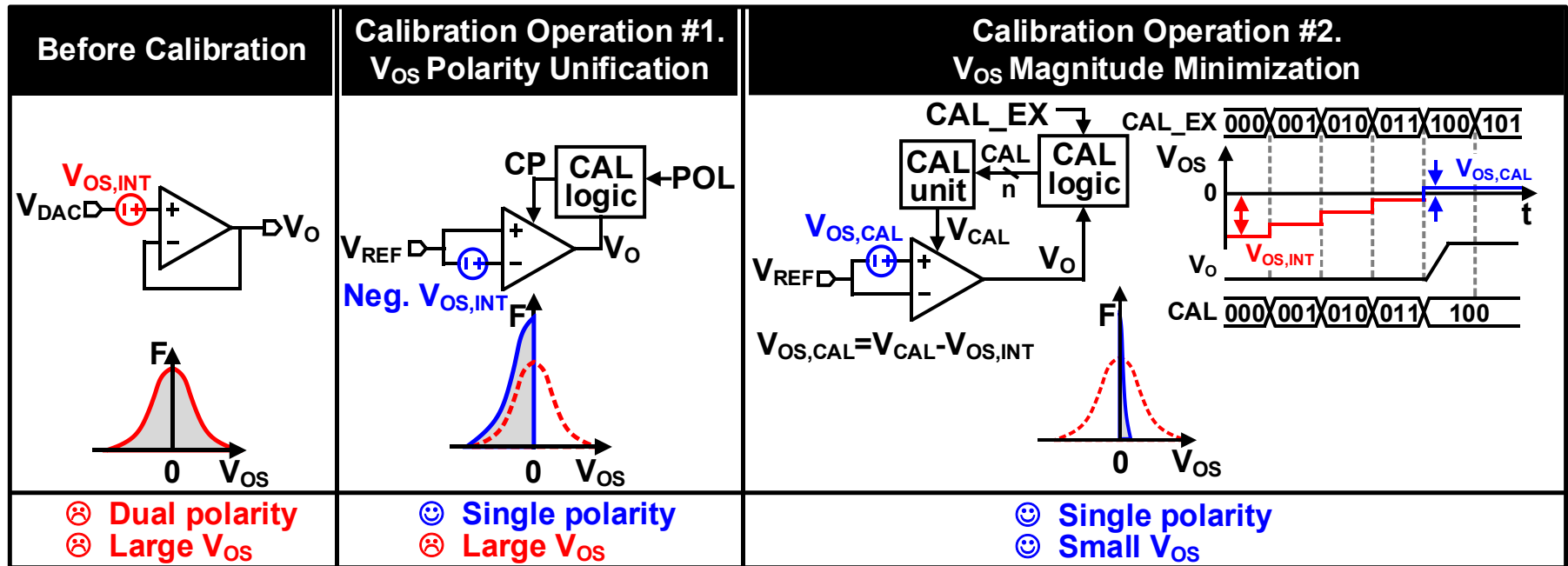


# Small-DVO SD-IC -Voltage Variation-



- Output voltage variation of SD-IC **degrades the image quality** of the display panel.
- Large deviation of voltage output (DVO) → non-uniform image

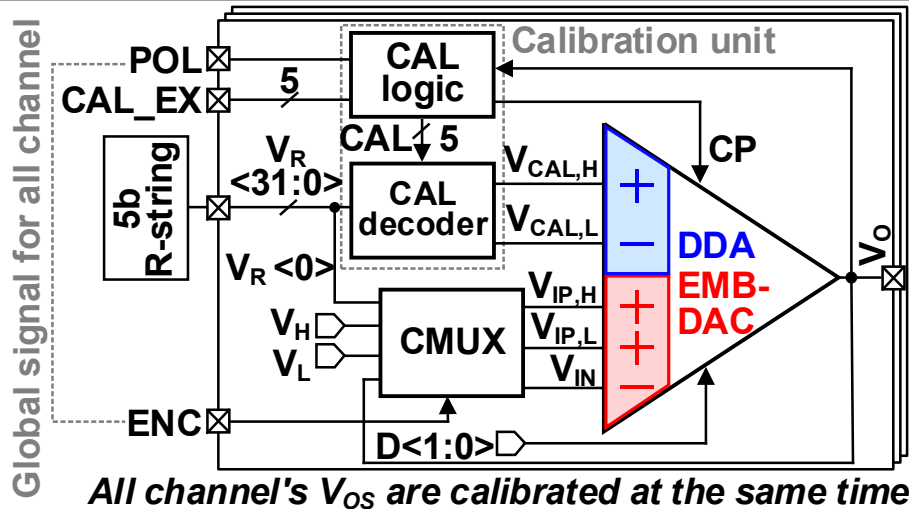
# Small-DVO SD-IC -Proposed Offset Calibration-



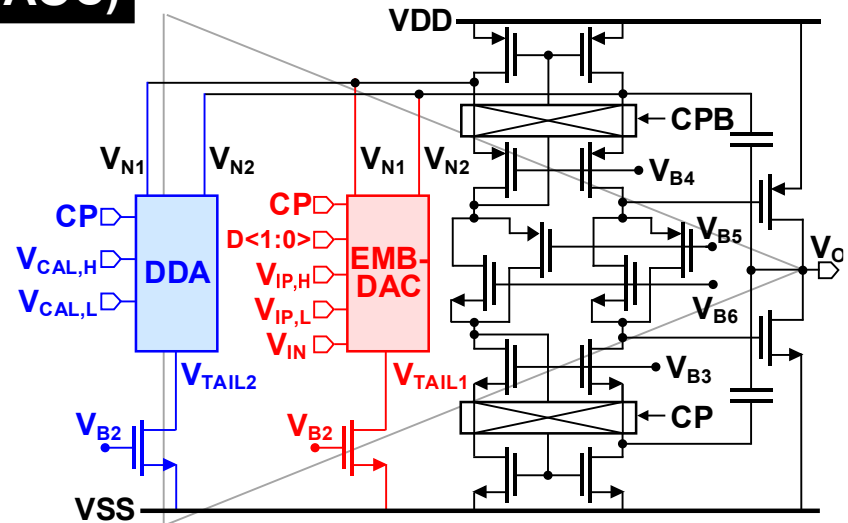
- The proposed calibration technique can reduce the random offset voltage.

# Small-DVO SD-IC -Implementation of ACAOC-

## All-channel automatic offset calibration (ACAOC)

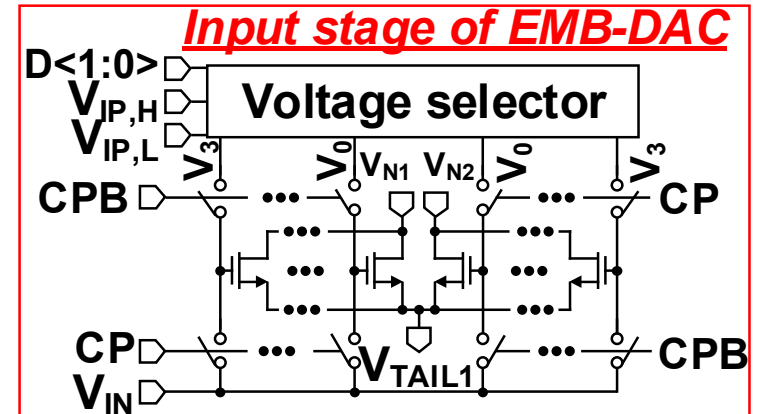
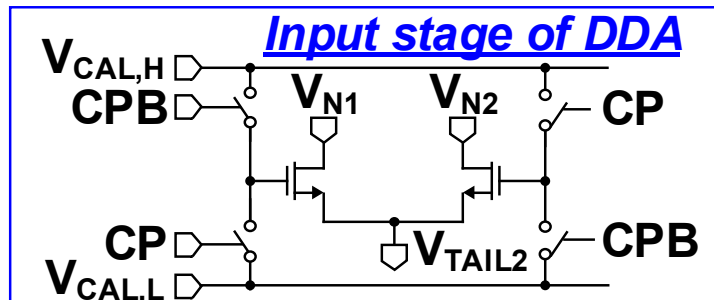


## Proposed core amplifier



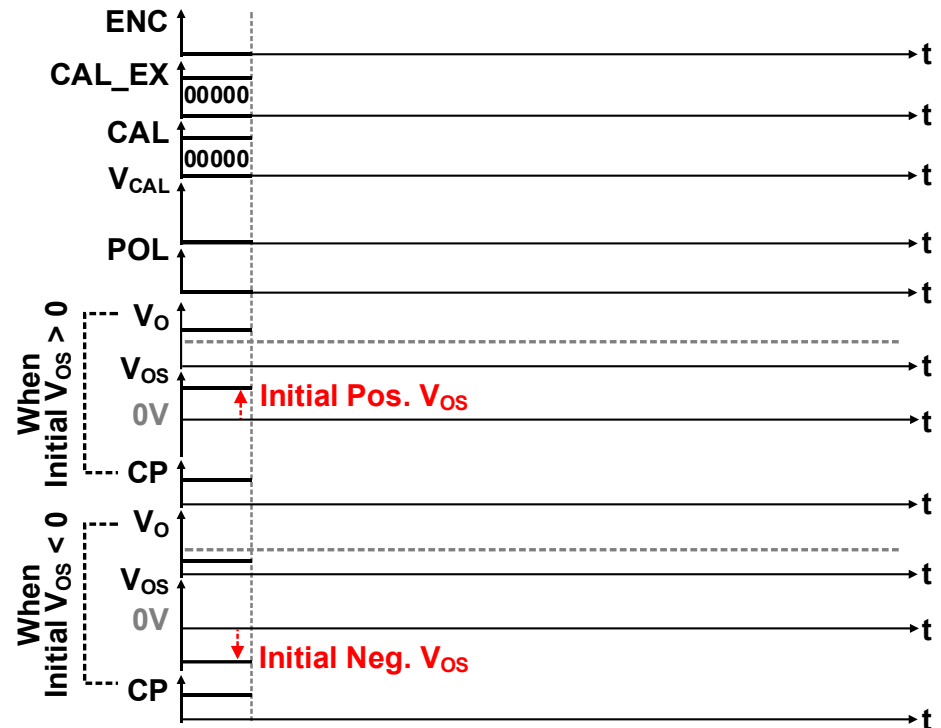
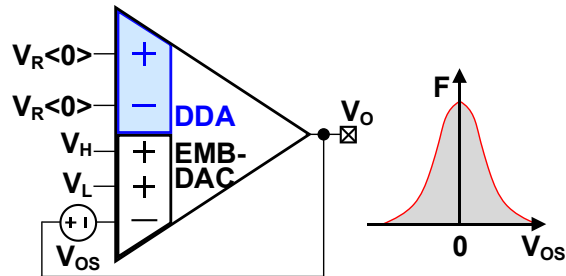
- All-channel automatic offset calibration (ACAOC)

- ☺ Single  $V_{Os}$  polarity
- ☺ Small  $V_{Os}$  magnitude



# Small-DVO SD-IC -ACAOC Operation(1/6)-

Phase#1: before calibration

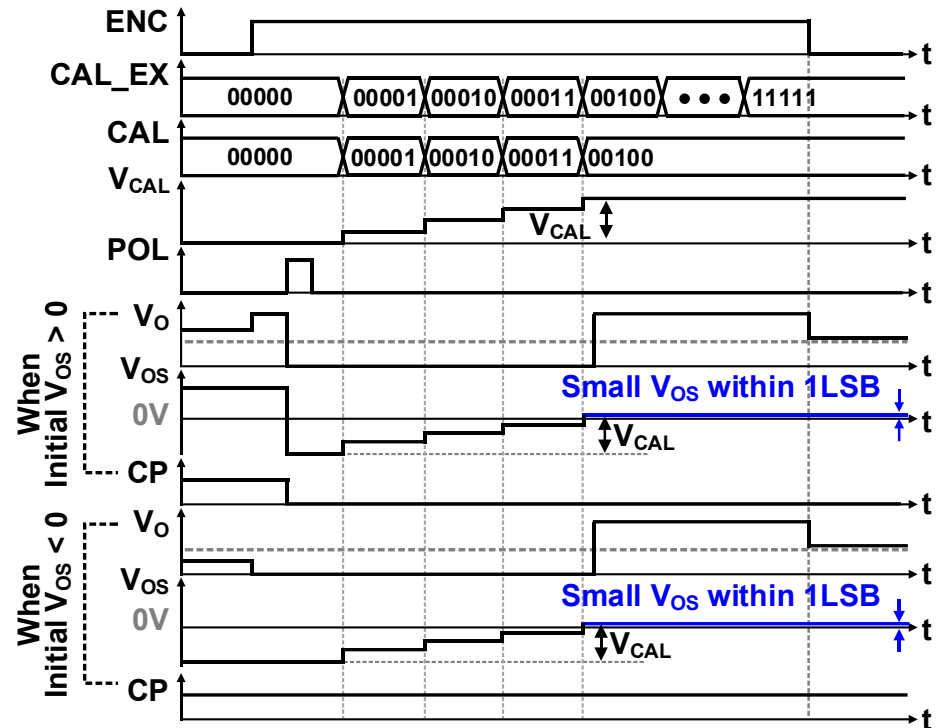
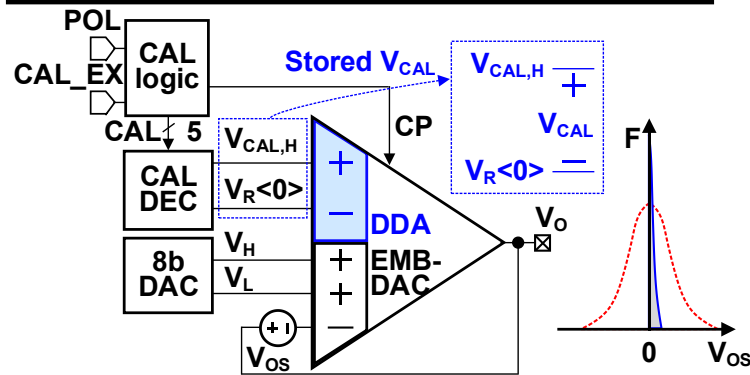


☹️ Dual polarity

☹️ Large  $V_{OS}$

# Small-DVO SD-IC -ACAOC Operation(6/6)-

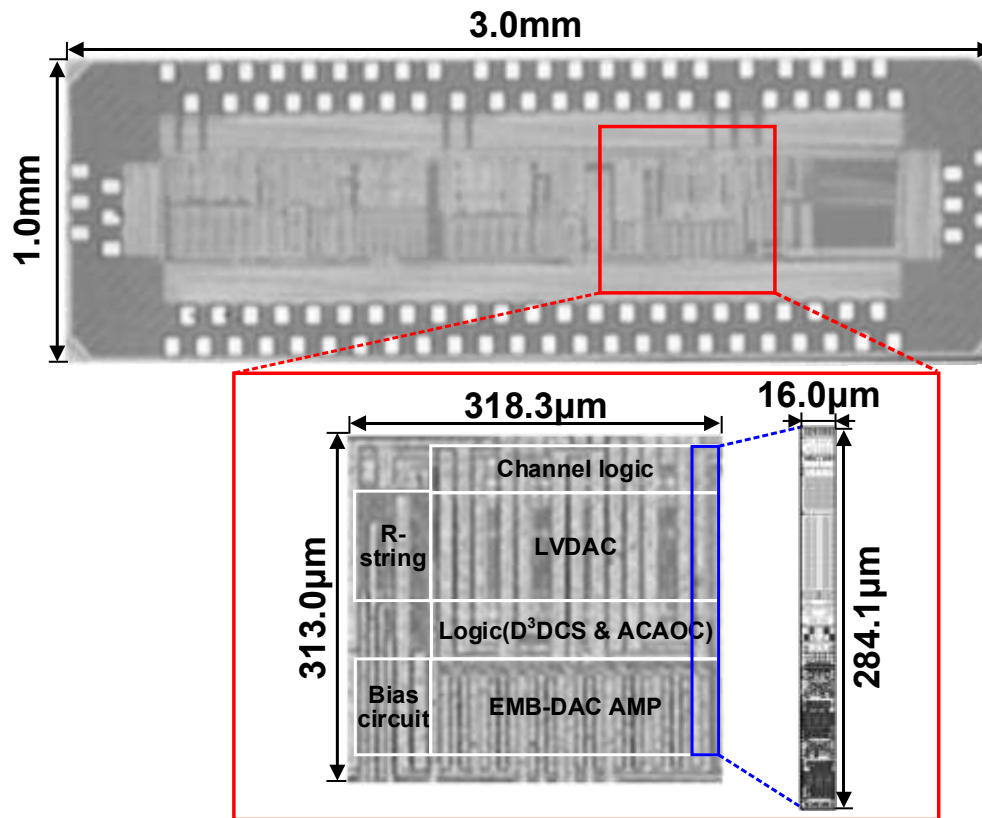
## Phase#4: display panel driving



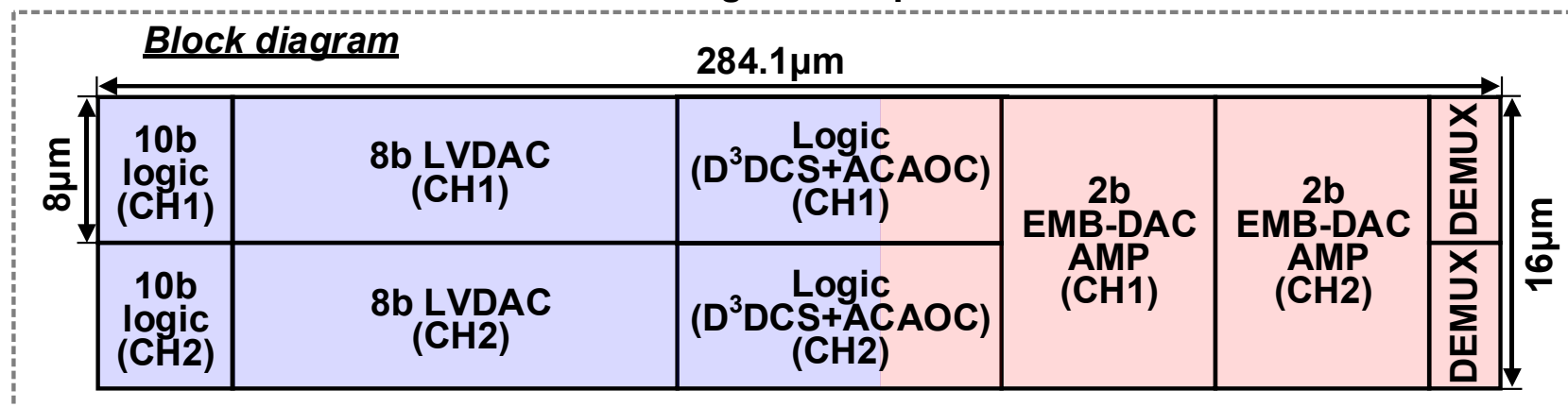
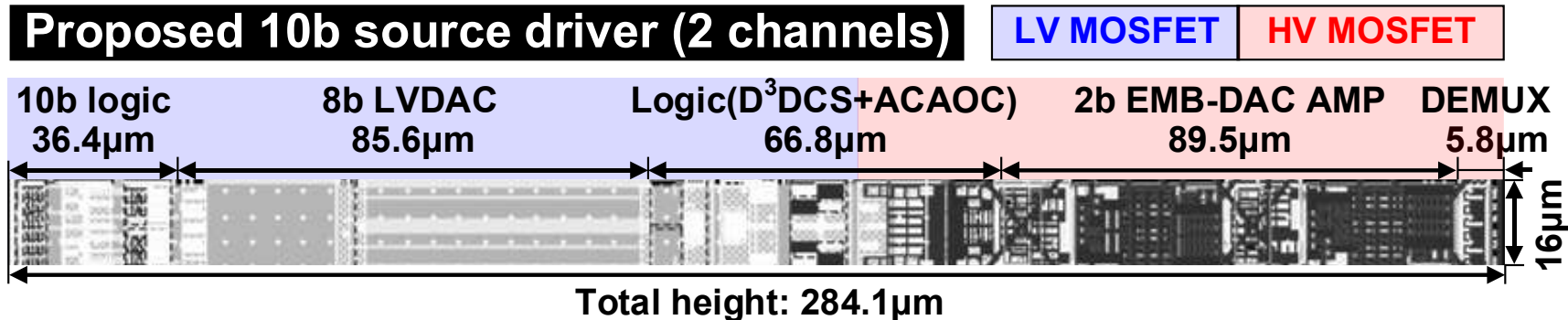
- ☺ Single polarity
- ☺ Small  $V_{OS}$

# Die Micrograph

- TSMC 65nm CMOS process

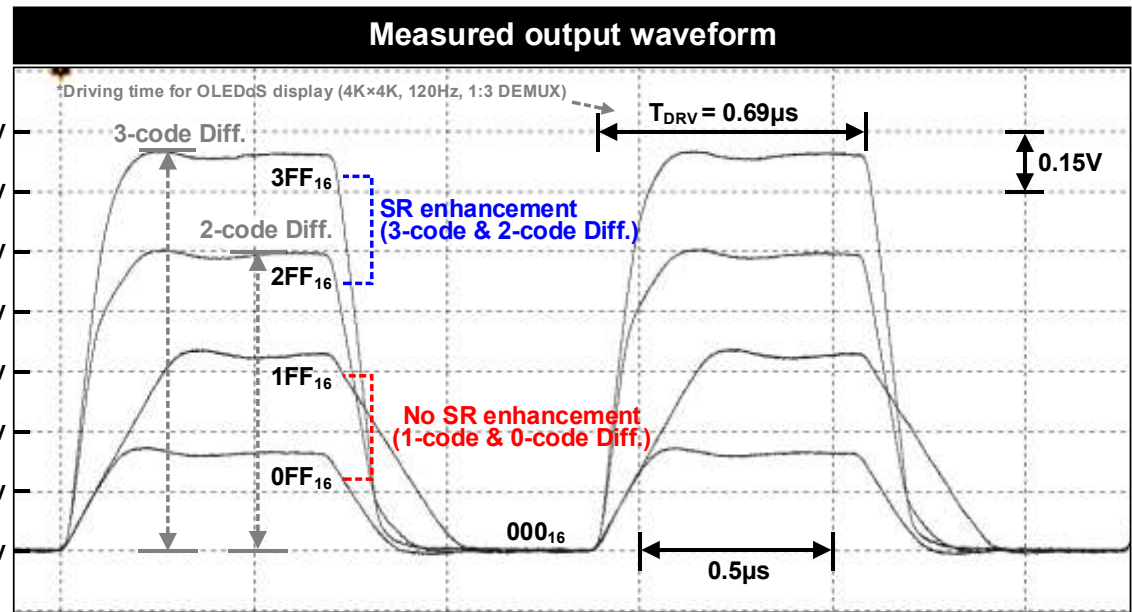
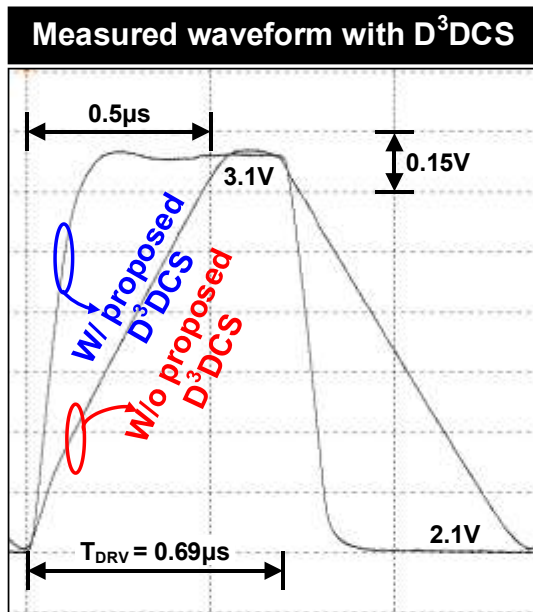


# Layout of Proposed SD-IC



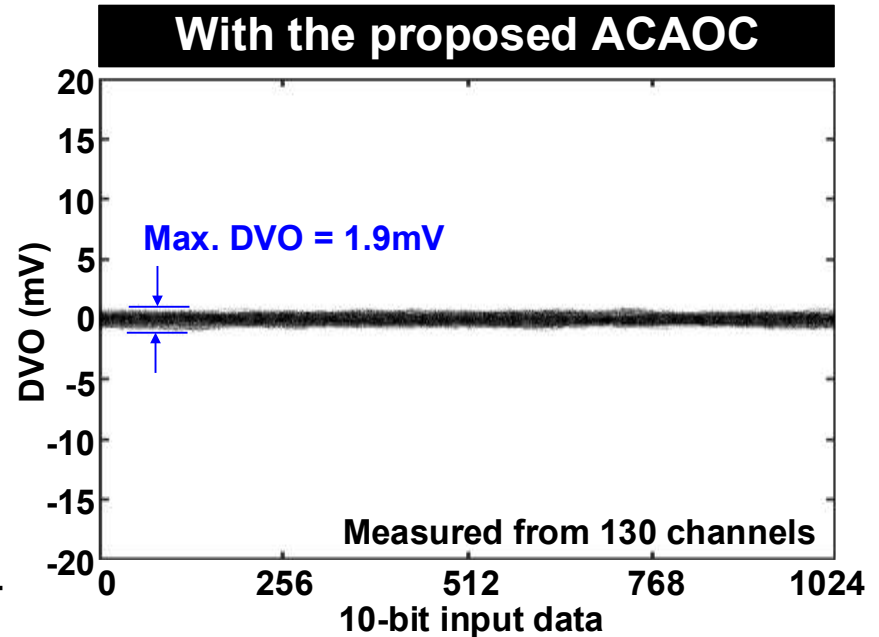
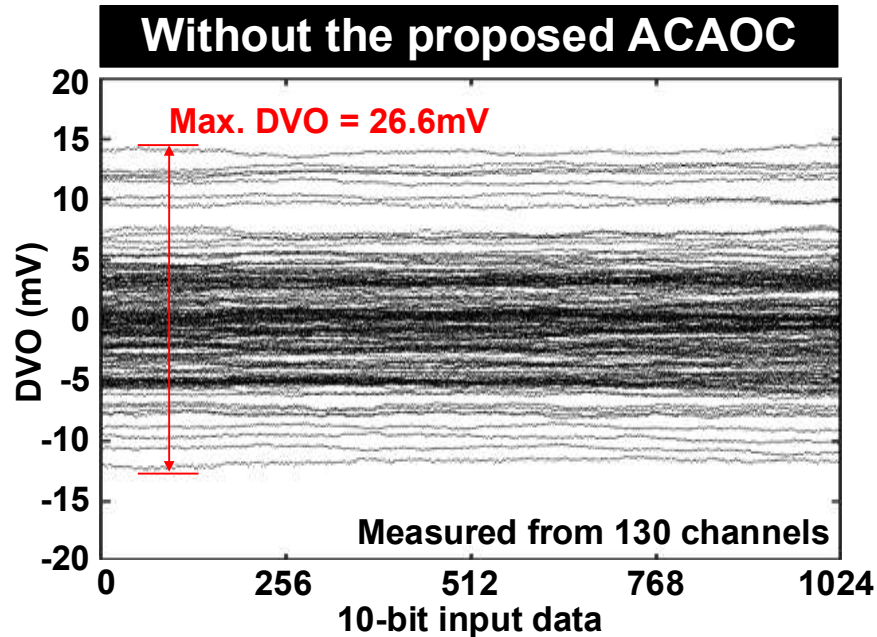
- Achieved 2,273μm<sup>2</sup>/channel → small area SD-IC

# Measured Waveforms



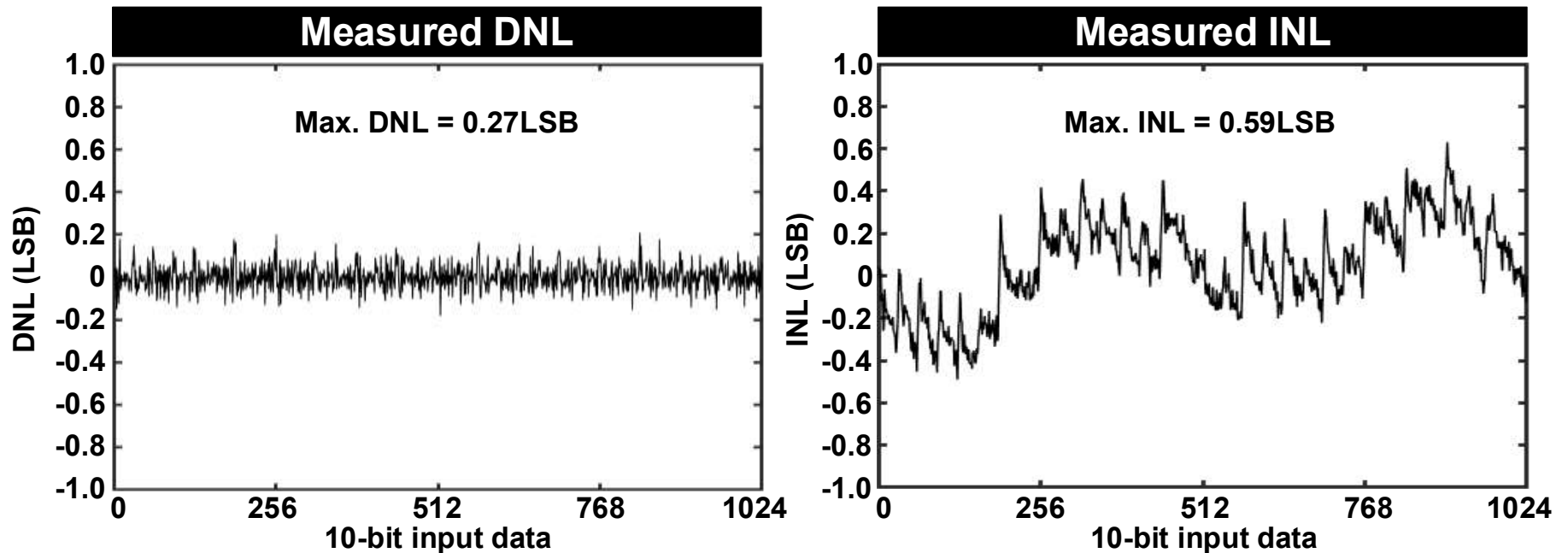
- Achieved a settling time of 0.69µs → fast SD-IC

# Measured DVO



- Achieved a DVO of 1.9mV → small DVO SD-IC

# Measured Linearity



- Achieved DNL/INL of 0.27/0.59 LSB, respectively.

# Performance Comparison

	J.-S.Kim JSSC 2021	G.-W.Lim JSSC 2023	S.Shin JSSC 2024	Y.Park ISSCC 2024	J.Ahn ISSCC 2024	This Work
Technology	90nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS	65nm CMOS	65nm CMOS
Application	OLED	OLED	OLED	OLED	OLED	OLEDoS (6285PPi)
Output range	0.2V to 4.8V	0.3V to 4.5V	0.1V to 4.9V	0.25V to 4.5V	0.3V to 4.7V	2.1V to 3.1V*
Gray scale	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
Gamma curve	Fully nonlinear	Linear	Piecewise linear	Piecewise linear	Fully nonlinear	Piecewise linear
Frame rate	-	60Hz	60Hz	240Hz	60Hz	120Hz
Panel resolution	-	2560 X 1600	2520 × 1080	3840 x 2160	3840 x 2160	4000 x 4000
DEMUX	-	-	-	-	-	1:3 DEMUX
DNL / INL	0.20/0.42LSB	0.39/0.90LSB	-0.39/1.17LSB	0.21/1.21LSB	0.49/0.85LSB	0.27/0.59LSB
Max. DVO	7.9mV (4.2x)	4.8mV (2.5x)	15.5mV (8.2x)	11.5mV (6.1x)	10.0mV (5.3x)	1.9mV (1.0x smallest)
Settling time	2.2μs (3.2x)	5.3μs (7.9x)	1.5μs (2.2x)	1.5μs (2.2x)	5.0μs (7.2x)	0.69μs (1.0x fastest)
R <sub>LOAD</sub> /C <sub>LOAD</sub>	30kΩ/30pF	30kΩ/30pF	3kΩ/100pF	3kΩ/100pF	30kΩ/30pF	10kΩ/10pF
Static current per channel	2.8μA	1.8μA	1.7μA	2.4μA	1.5μA	5.4μA
Channel area (1CH)	5328μm <sup>2</sup> (296.0 × 18.0μm <sup>2</sup> ) (2.3x)	2688μm <sup>2</sup> (168.0 × 16.0μm <sup>2</sup> ) (1.2x)	4065μm <sup>2</sup> (243.4 × 16.7μm <sup>2</sup> ) (1.8x)	4815μm <sup>2</sup> (321.0 × 15.0μm <sup>2</sup> ) (2.1x)	2411μm <sup>2</sup> (150.7 × 16.0μm <sup>2</sup> ) (1.1x)	2273μm <sup>2</sup> (142.1 × 16.0μm <sup>2</sup> ) (1.0x smallest)
Channel area (2CH)	10656μm <sup>2</sup> (592.0 × 18.0μm <sup>2</sup> ) (2.3x)	5376μm <sup>2</sup> (336.0 × 16.0μm <sup>2</sup> ) (1.2x)	8130μm <sup>2</sup> (486.8 × 16.7μm <sup>2</sup> ) (1.8x)	9630μm <sup>2</sup> (642.0 × 15.0μm <sup>2</sup> ) (2.1x)	4822 μm <sup>2</sup> (301.4 × 16.0μm <sup>2</sup> ) (1.1x)	4546μm <sup>2</sup> (284.1 × 16.0μm <sup>2</sup> ) (1.0x smallest)

\*Output range for OLEDoS pixel circuit with PMOS driving TR

# Summary

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- Small area, fast, and small DVO SD-IC is required for OLEDoS display.
- **Small area SD-IC** is achieved using LVDAC, DEMUX, and two-stage DAC architecture, resulting in a channel area of **2273 $\mu\text{m}^2$** .
- **Fast SD-IC** is implemented by D<sup>3</sup>DCS, achieving a settling time of less than **0.69 $\mu\text{s}$** .
- **Small DVO SD-IC** is realized by ACAOC, reducing DVO to less than **1.9mV**.
- The proposed SD-IC is well-suited for OLEDoS displays.

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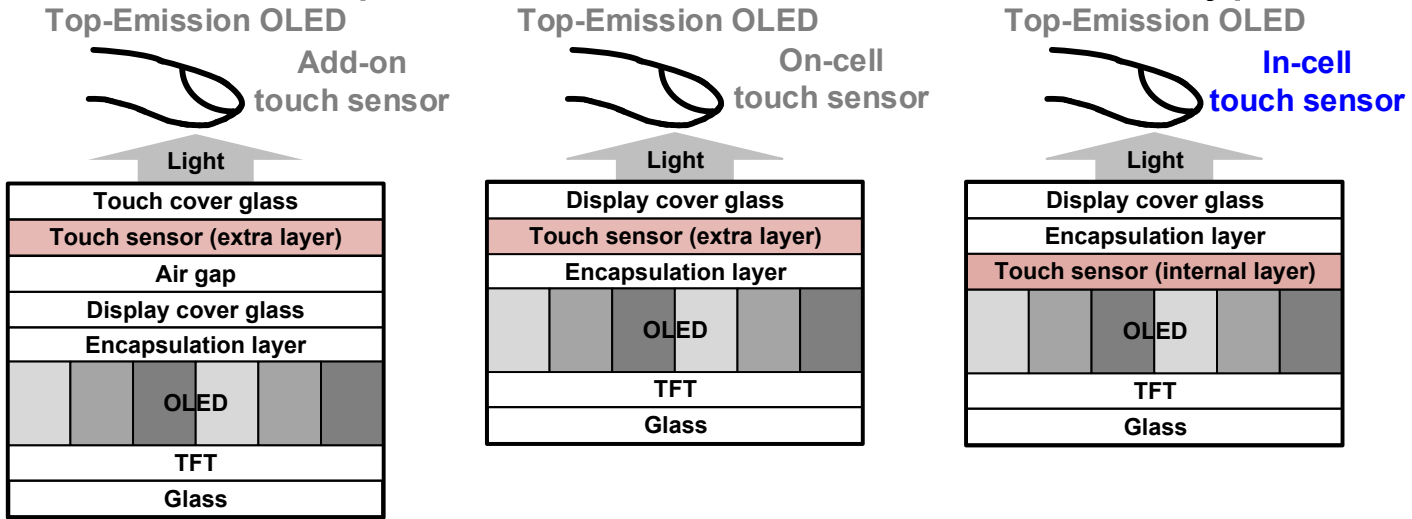
[연구분야: 센서 회로]

# Touch Sensor

# Background



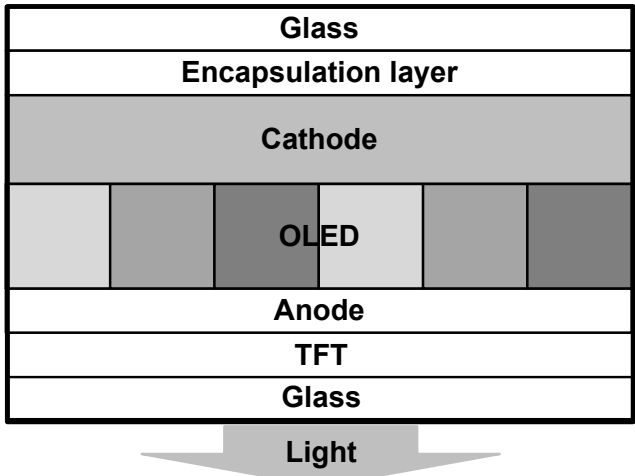
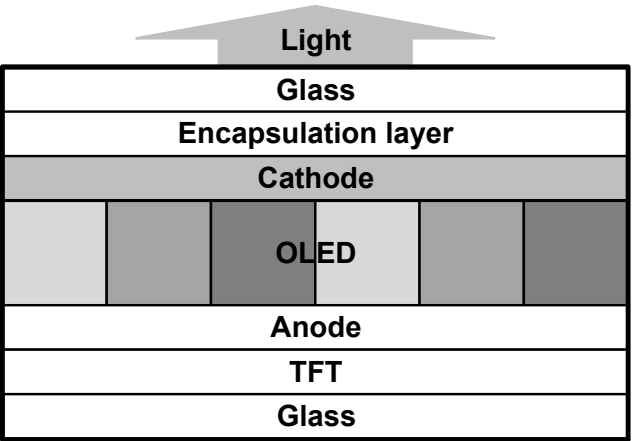
# Background - Top-Emission OLED Touch Sensor Type-



Add-on touch sensor	On-cell touch sensor	In-cell touch sensor
☺ <b>SNR</b> ↑ (near finger)	☹ <b>SNR</b> ↓ (far from finger & near DDI)	☹ <b>SNR</b> ↓ (far from finger & near DDI)
☹ <b>Luminance</b> ↓ (air gap → visual issue)	☺ <b>Luminance</b> ↑ (no air gap)	☺ <b>Luminance</b> ↑ (no external sensor layer)
☹ <b>Manufacturing cost</b> ↑ (additional sensor layer)	☹ <b>Manufacturing cost</b> ↑ (no air gap)	☺ <b>Manufacturing cost</b> ↓ (no external sensor layer)

## Advantages of in-cell touch sensor

# Background - Top-Emission OLED vs Bottom-Emission OLED-



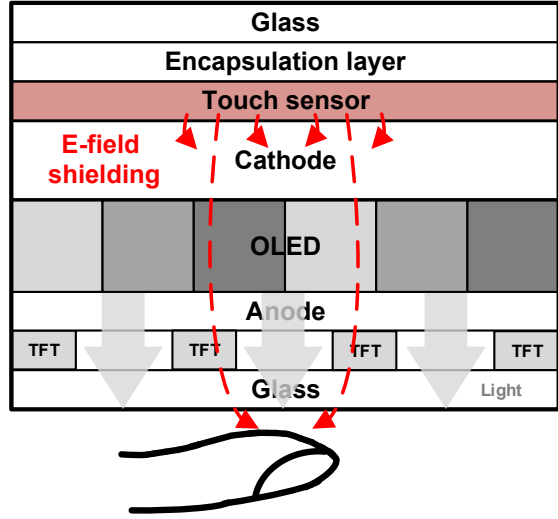
Top-emission OLED	Bottom-emission OLED
<p>☹ <b>Manufacturing cost</b> ↑ (transparent cathode → costly material)</p>	<p>☺ <b>Manufacturing cost</b> ↓ (opaque cathode → cheaper material)</p>
<p>☹ <b>Luminance</b> ↓ (thin cathode → high sheet R → current injection ↓)</p>	<p>☺ <b>Luminance</b> ↑ (thick cathode → low sheet R → current injection ↑)</p>

**Advantages of bottom-emission OLED**

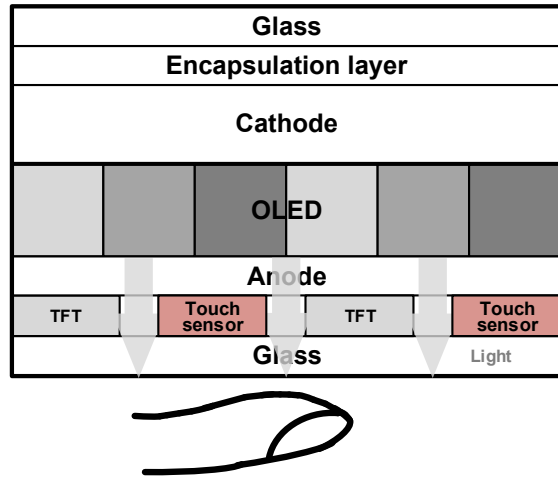
# Background

-Challenges of In-Cell Touch Sensor for Bottom-Emission OLED-

Primitive Bottom-Emission & In-Cell Type 1



Primitive Bottom-Emission & In-Cell Type 2



Type 1	Type 2
⊗ SNR↓ (E-field is shielded by cathode layer)	⊗ Luminance↓ (aperture ratio↓)

A new in-cell touch sensor suitable for bottom-emission OLED is needed.

# Background

-Summary of OLED Displays and Touch Sensor Type-

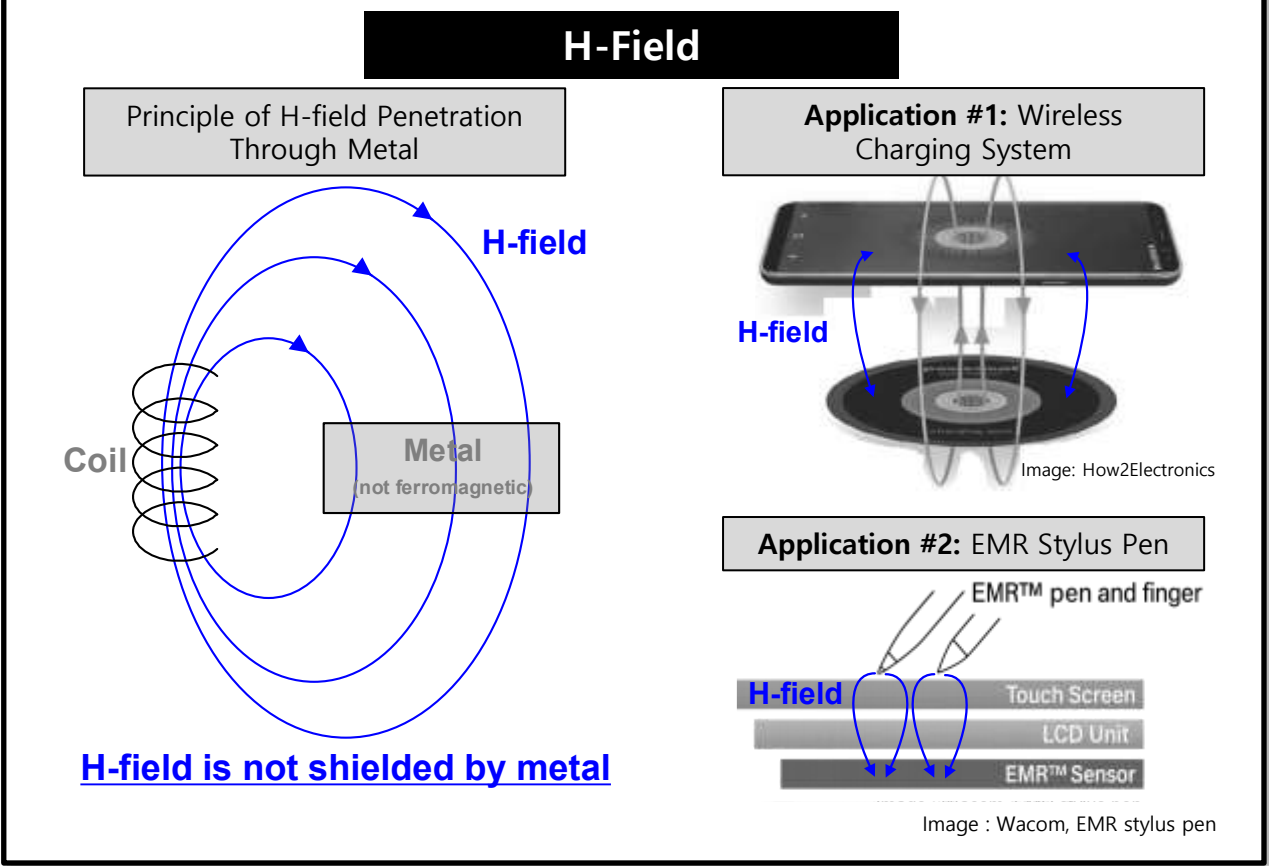
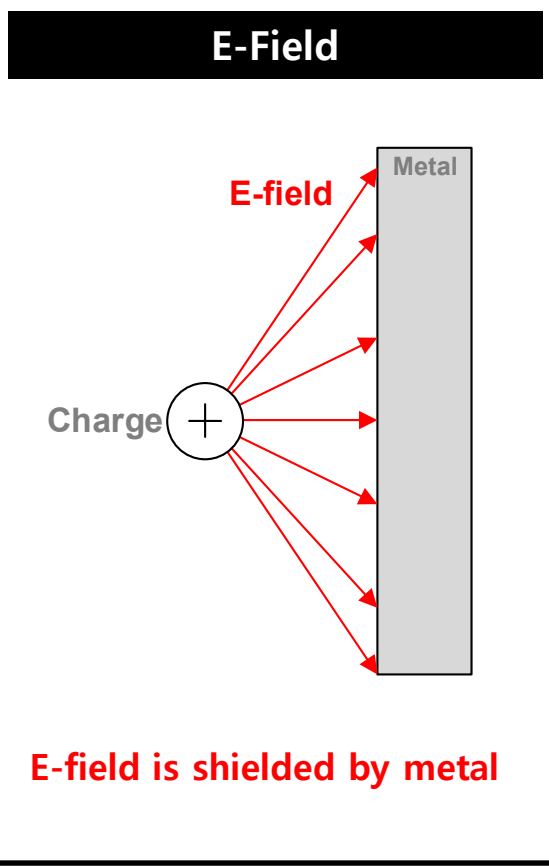
Top-emission OLED			Bottom-emission OLED		
☹️ MFG. cost ↑ ☹️ Luminance ↓			😊 MFG. cost ↓ 😊 Luminance ↑		
Add-on touch sensor	On-cell touch sensor	In-cell touch sensor	In-cell touch sensor (E-field)		In-cell touch sensor (H-field)
			Type1	Type2	This work
☹️ MFG. cost ↑	☹️ MFG. cost ↑	😊 MFG. cost ↓	☹️ SNR ↓	☹️ Luminance ↓	😊 MFG. cost ↓ 😊 Luminance ↑ 😊 SNR ↑
☹️ Luminance ↓	😊 Luminance ↑	😊 Luminance ↑			

This work combines  
**bottom-emission OLED & in-cell touch sensor**

😊 Manufacturing cost  
 ↓  
 😊 Luminance ↑

😊 Manufacturing cost  
 ↓  
 😊 Luminance ↑

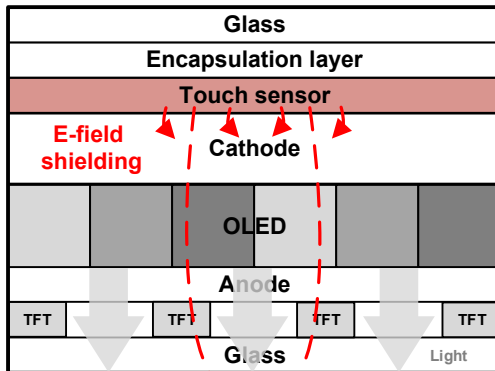
# Background - E-field vs H-field -



# Architecture of Proposed LLC Touch Sensor

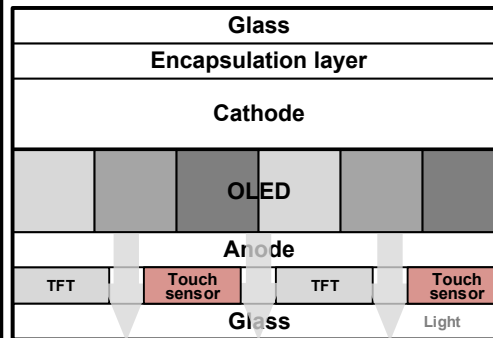
## Bottom-Emission OLED with In-Cell Touch Sensor (E-Field)

Type 1



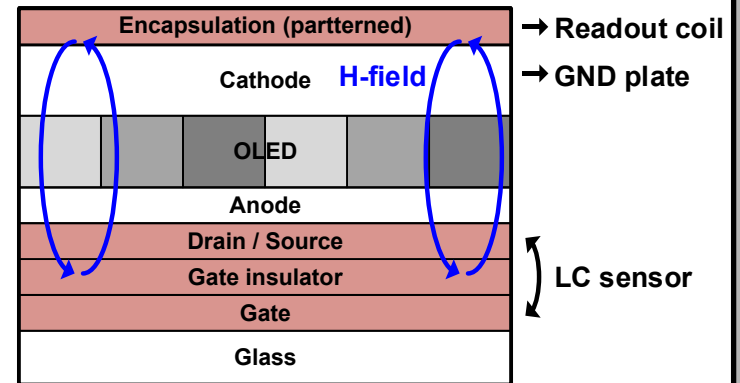
☹️ SNR ↓

Type 2



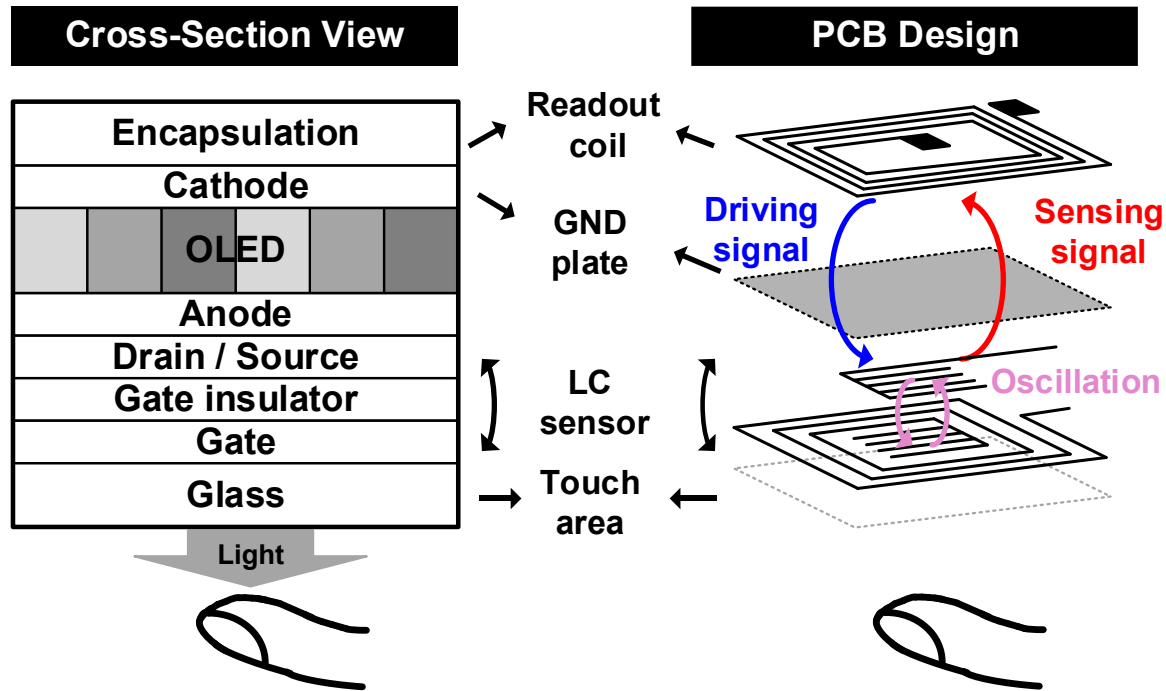
☹️ Luminance ↓

## Bottom-Emission OLED with In-Cell Touch Sensor (H-Field)



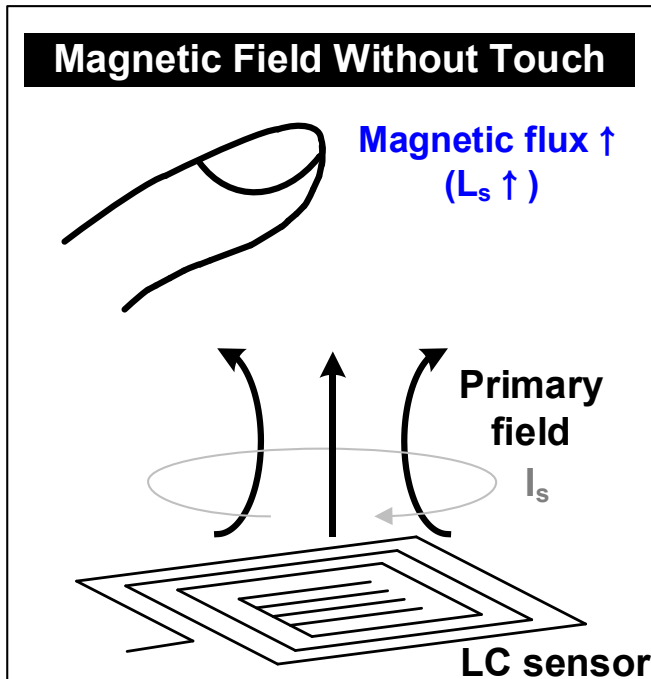
- ☺️ Manufacturing cost ↓
- ☺️ Luminance ↑
- ☺️ SNR ↑

# Principle of Operation

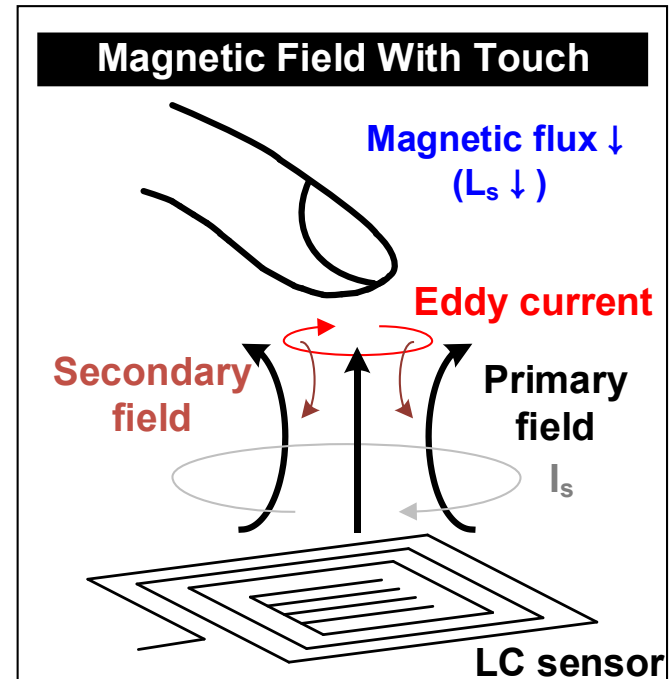


- **Driving / sensing signal** via inductive coupling (LC sensor  $\rightleftharpoons$  readout coil)
- **Resonance** by L and C in the LC sensor

# Analysis of Characteristics -Inductance-

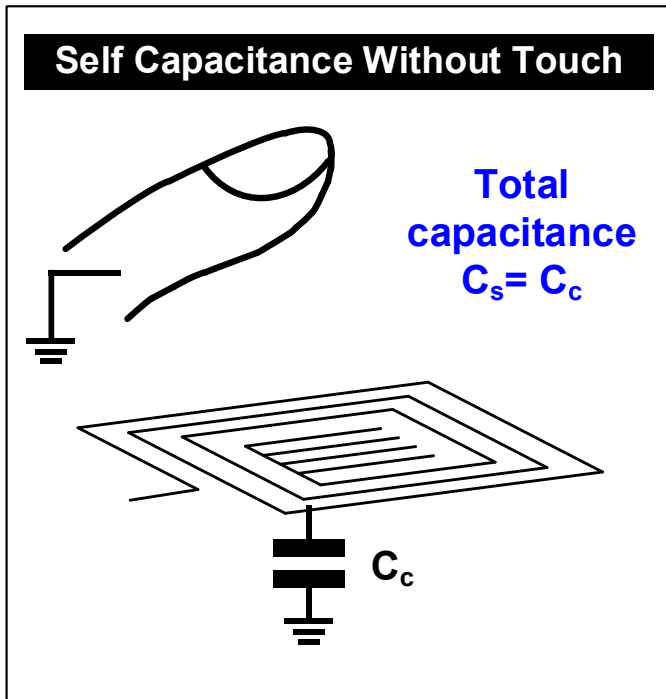


Inductance formed by primary magnetic field

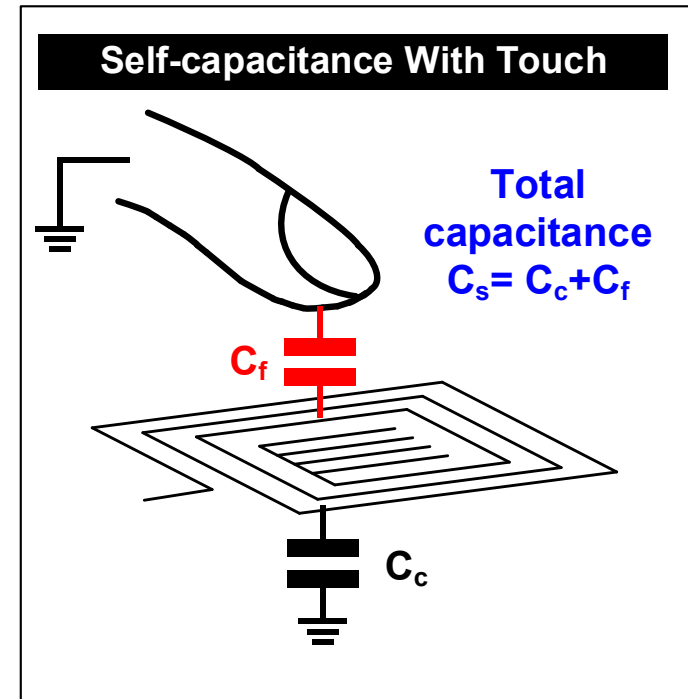


Eddy current reduces inductance ( $L_s \downarrow$ )

# Analysis of Characteristics -Capacitance-



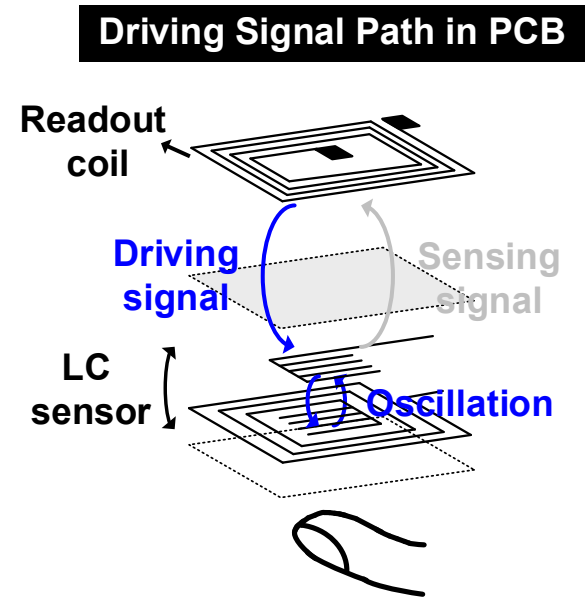
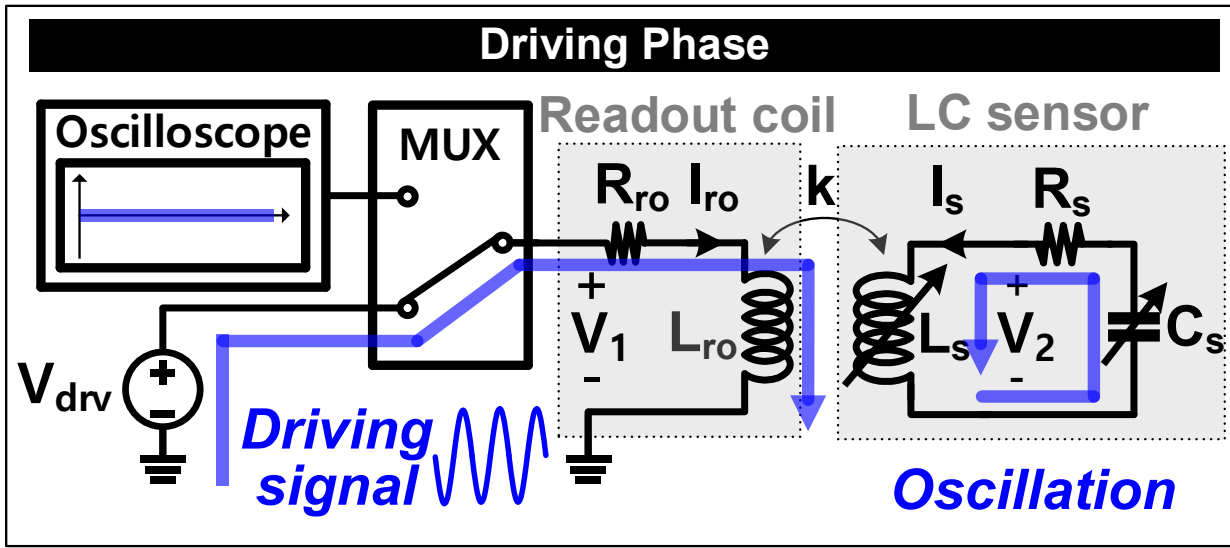
Baseline self-capacitance



Finger-induced  $C_f$  is added  $\rightarrow C_s$

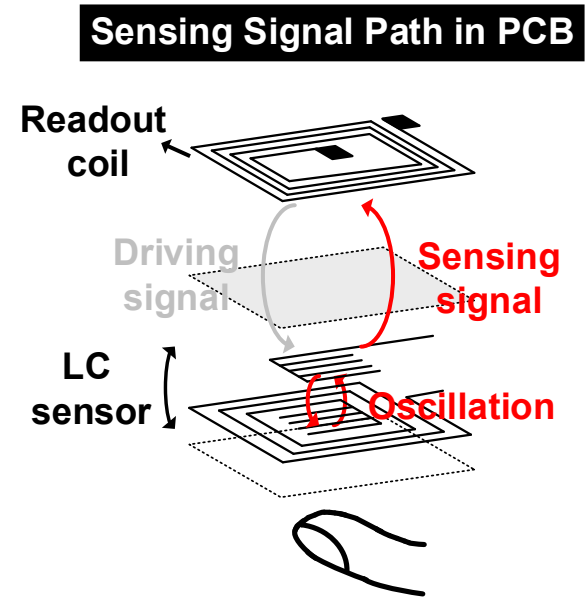
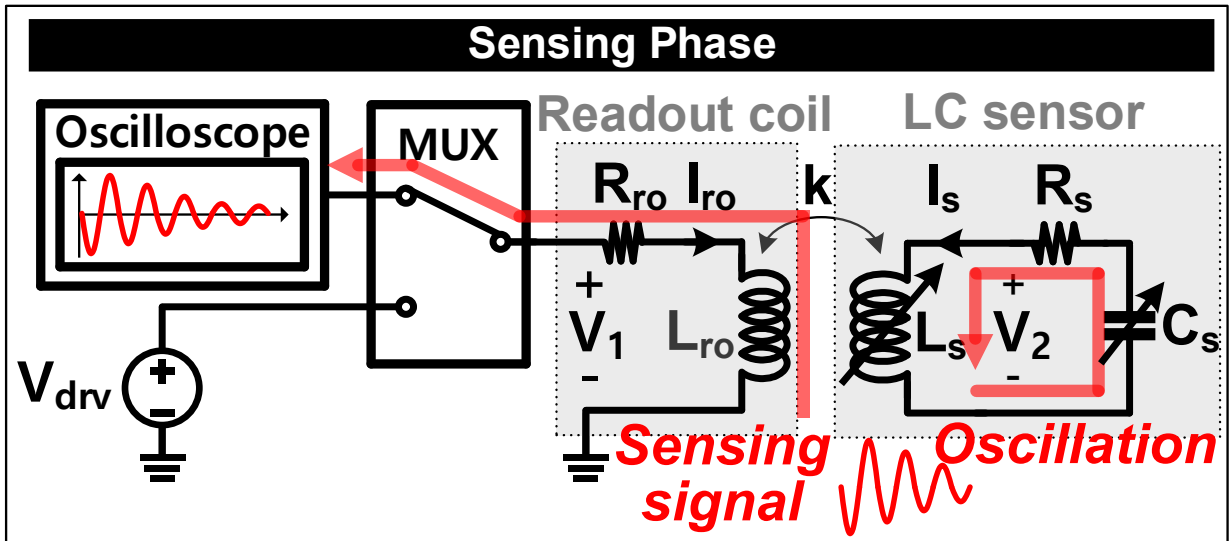


# Driving & Sensing Method -Driving Phase-



- $V_{DRV} \rightarrow L_{ro}$  via MUX
- Inductive coupling :  $L_{ro} \rightarrow L_s$

# Driving & Sensing Method -Sensing Phase-



- MUX links sensing signal to oscilloscope
- Touch:  $L_s$  decrease,  $C_s$  increase  $\rightarrow$  sensing signal change

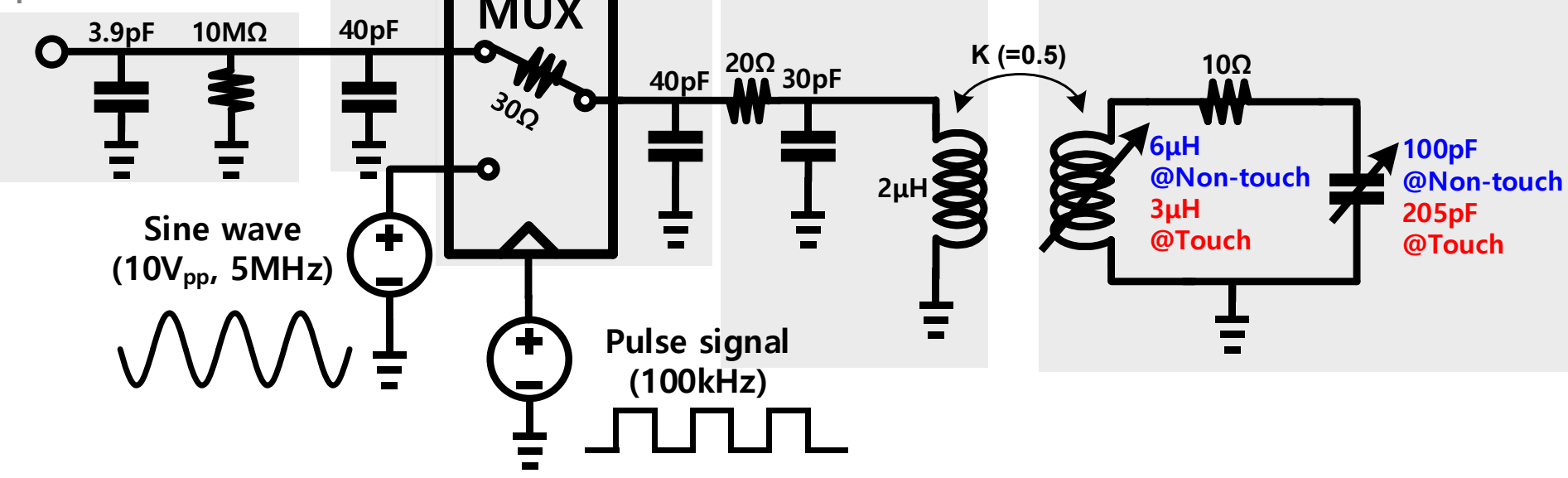
# Proposed LLC Touch Sensor -Simulation Condition-

Oscilloscope probe model

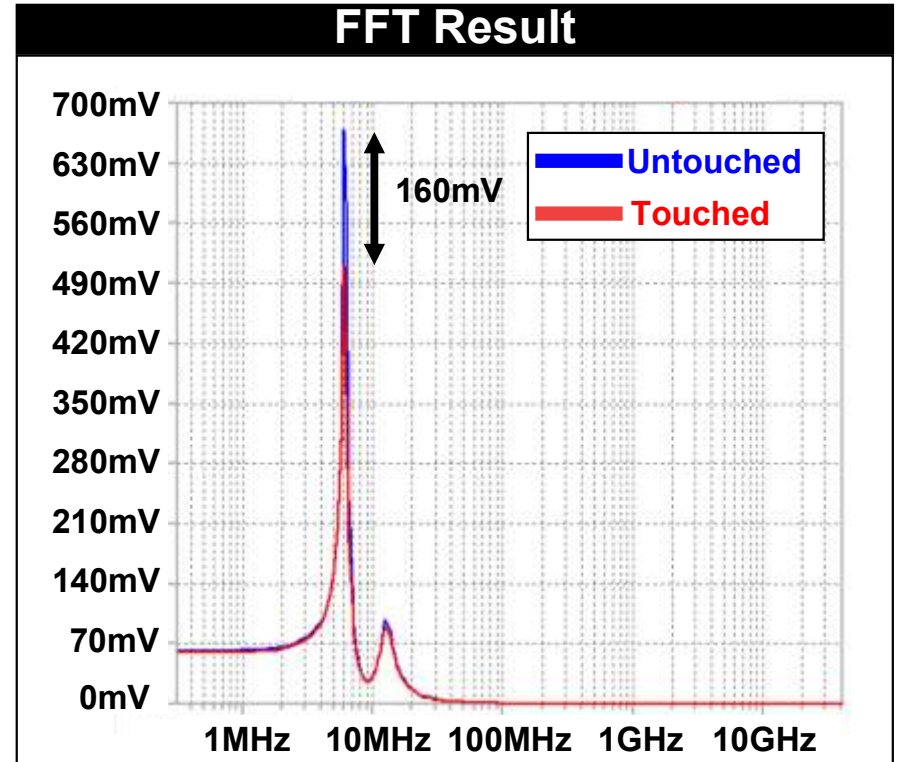
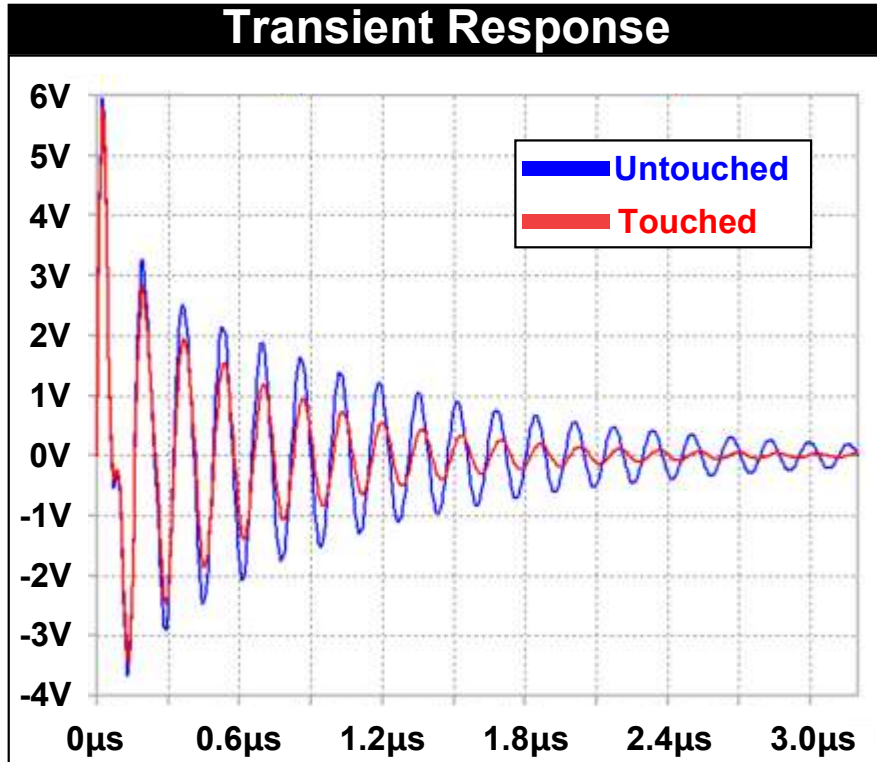
MUX model

Readout coil

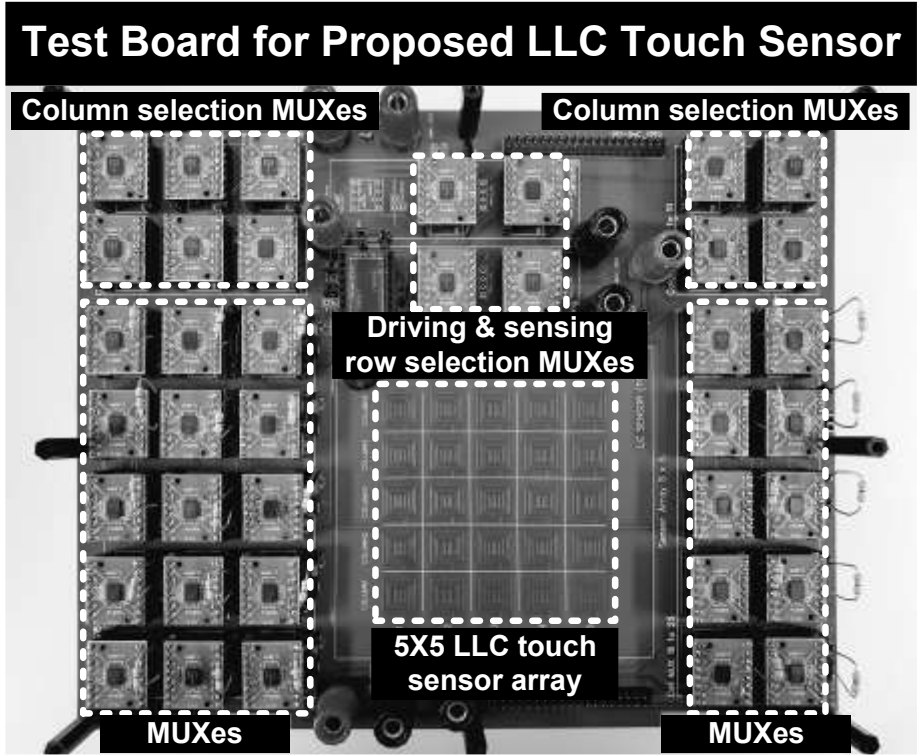
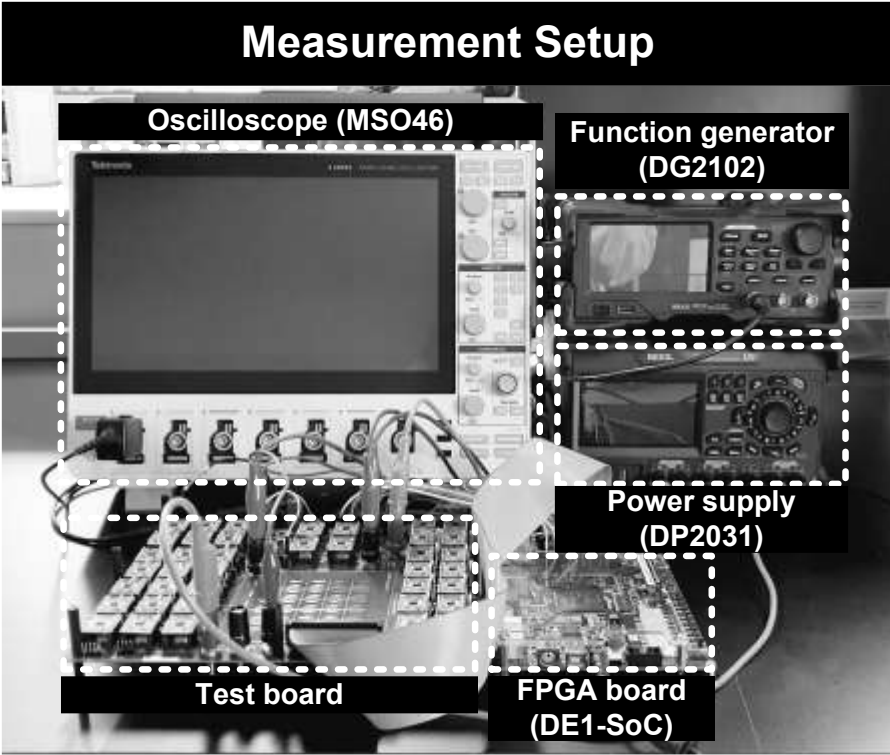
LC sensor



# Proposed LLC Touch Sensor -Simulation Result-

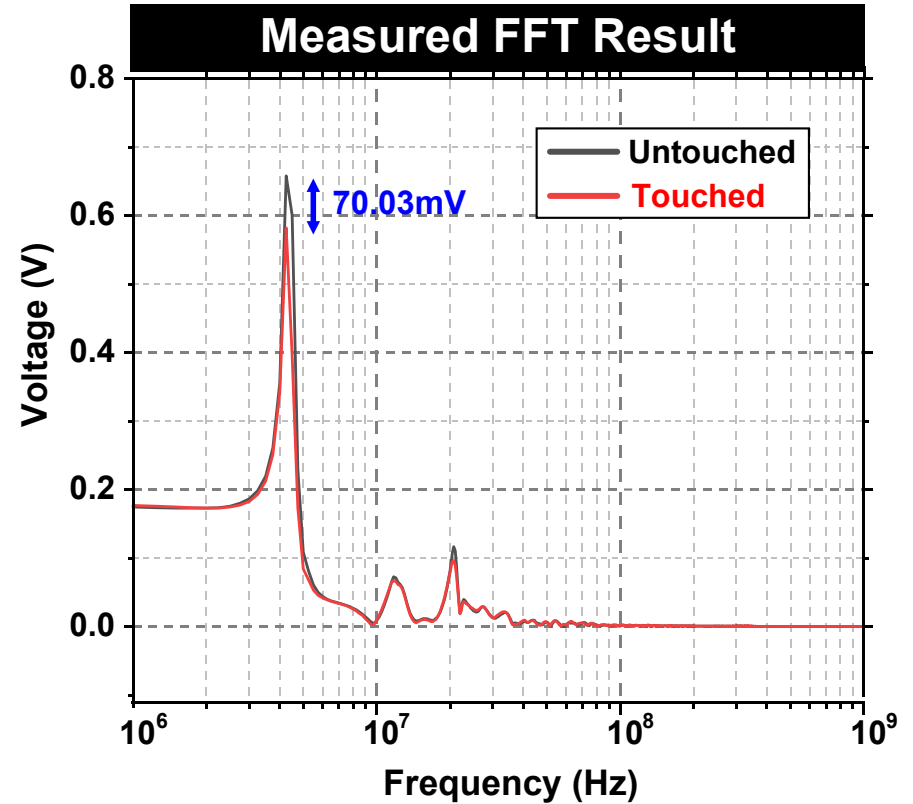
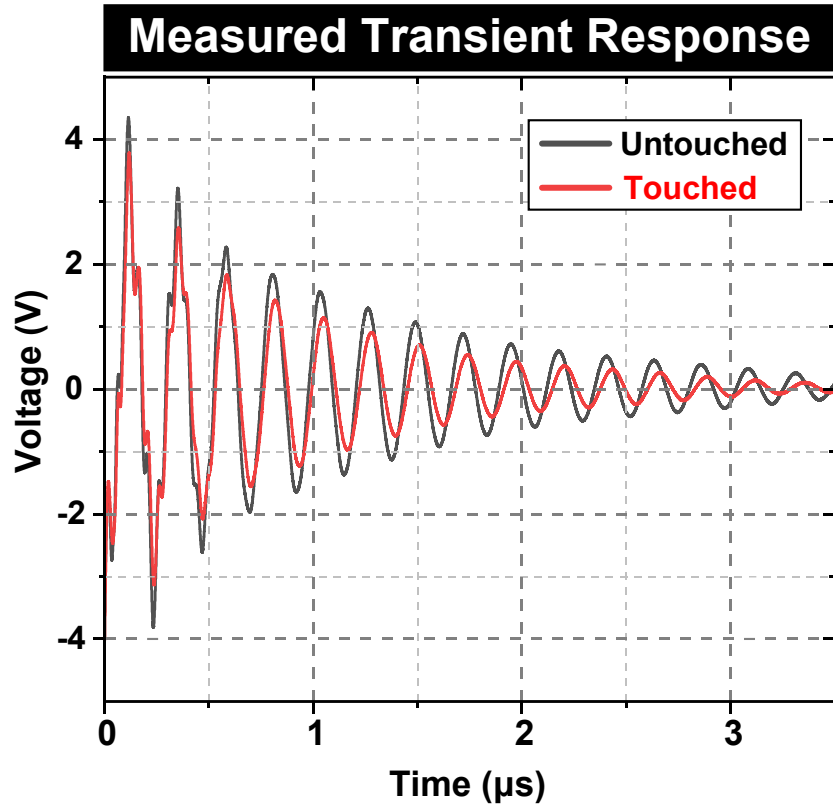


# Measurement Result -Measurement Setup-

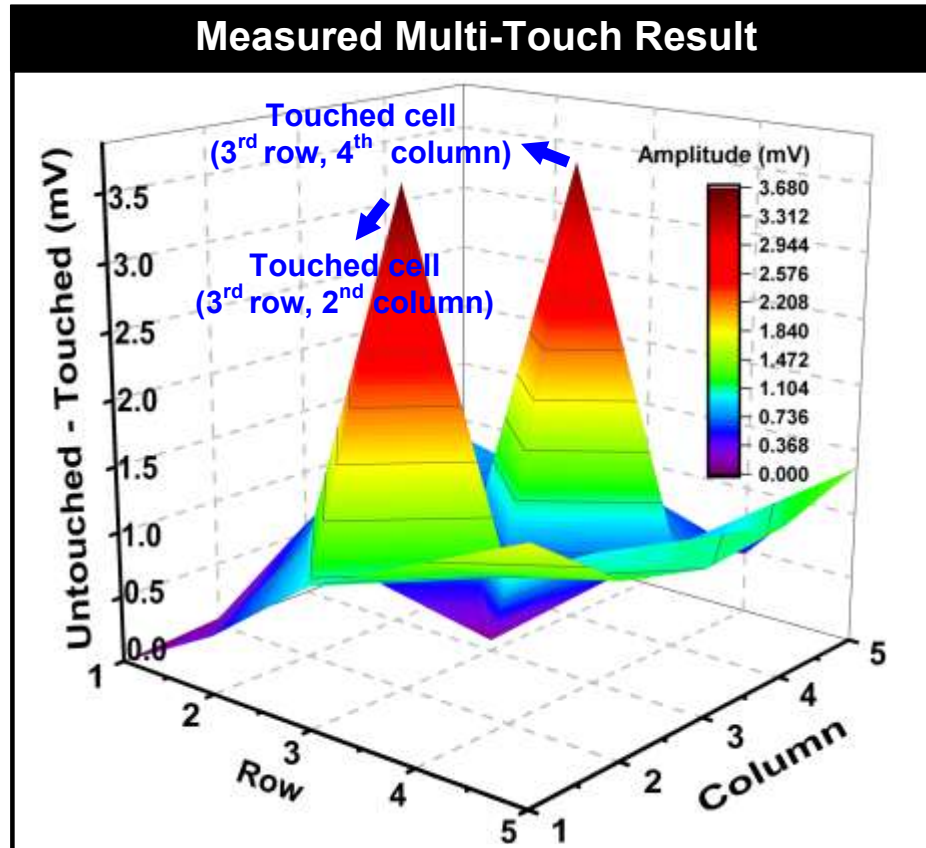


# Measurement Result

-Single-Sensor-



# Measurement Result - Measured Profile Image-



This measurement result was obtained using the revised PCB.

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[연구분야: 전원관리 회로]

# Touch Sensor

# Power Circuit Researches

## [ Switched-Inductor Power Supply Circuit]

### 1. Automotive 용 PMIC

- 40V Buck-boost converter 및 전용 gate driver IC Chip 개발 (BCD Process)
- 40V Buck converter 및 전용 gate driver IC Chip 개발 (BCD Process)

### 2. 저전력 IoT 용 PFM buck converter

- 저리플, 고효율 특성을 동시에 갖는 PFM buck converter 개발
- Ripple < 2mV, Efficiency >82%, Maximum Efficiency > 93%, IOU=100mA)

### 3. Mobile용 고효율 buck-boost converter (AICSP 2016)

- 입력 전압 변화에 따른 Mode-selection 기능 → battery 사용시간 증가

### 4. (ongoing) 저리플, 높은 효율을 동시에 갖는 OLED ELVSS용 PFM buck-boost converter

- Output voltage ripple : 1 mV, Max. efficiency 95%, PFM control

## [ Switched-Capacitor Power Supply Circuit ]

### 5. 4D 320단 NAND Flash Memory 양산제품용 고효율/고속 charge pump (@SK Hynix)

- 세계 최고 효율 variable-stage charge pump 개발 (30V charge pump, 8V charge pump)

### 6. 4D 128단 NAND Flash Memory 양산 제품용 고효율 negative charge pump (@SK Hynix)

- Charge pump stage 개선 및 charge pump controller 개선

## [ Linear regulator ]

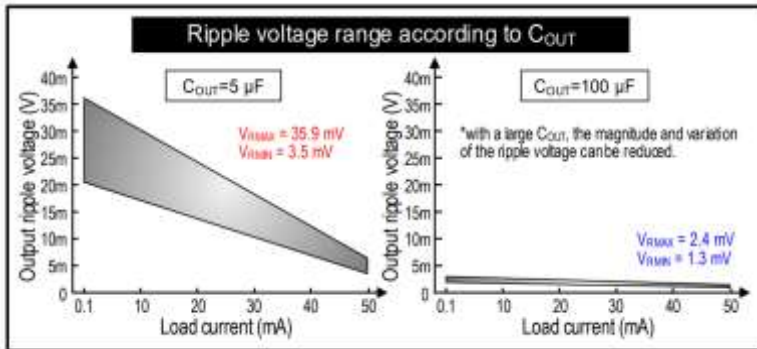
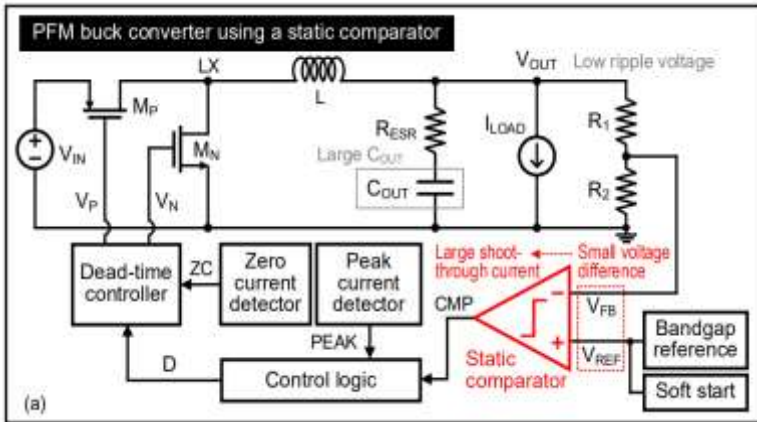
### 7. Volage Droop 개선한 Capacitorless LDO

# 1. 저전력 IoT 용 PFM buck converter

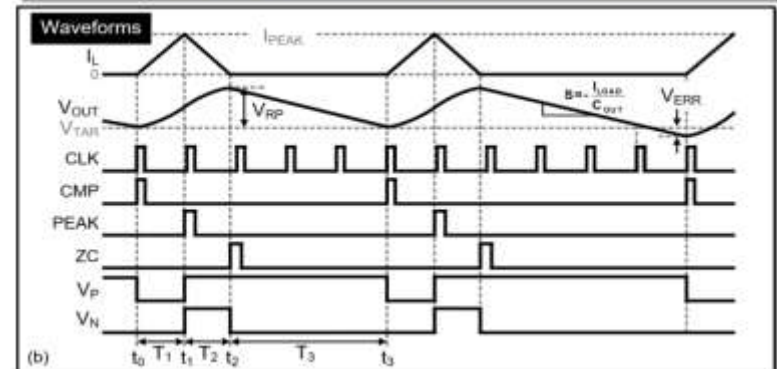
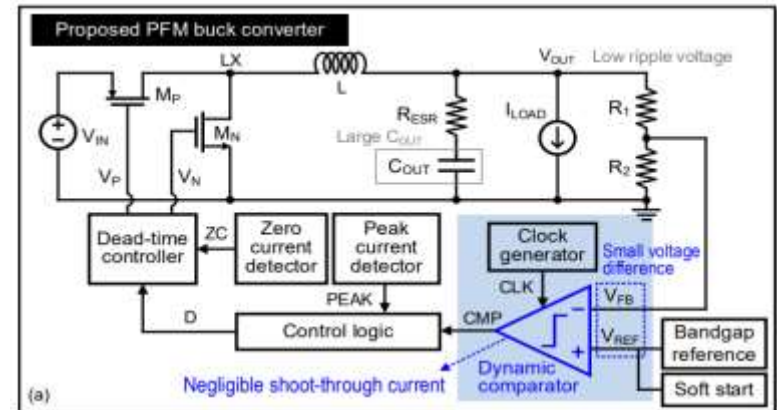
- A High-Light-Load-Efficiency, Low-Ripple-Voltage PFM Buck Converter for IoT Applications
- IEEE Transactions on Power Electronics (IF: 5.967) 2022

고효율 및 저리플 특성을 동시에 갖는 **PFM buck converter** 개발

Conventional PFM buck converter  
Tradeoff between Efficiency and Ripple



Proposed PFM buck converter  
breaks the tradeoff (Efficiency and Ripple)

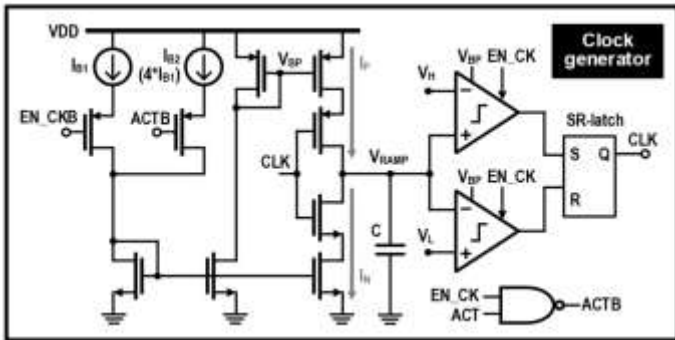
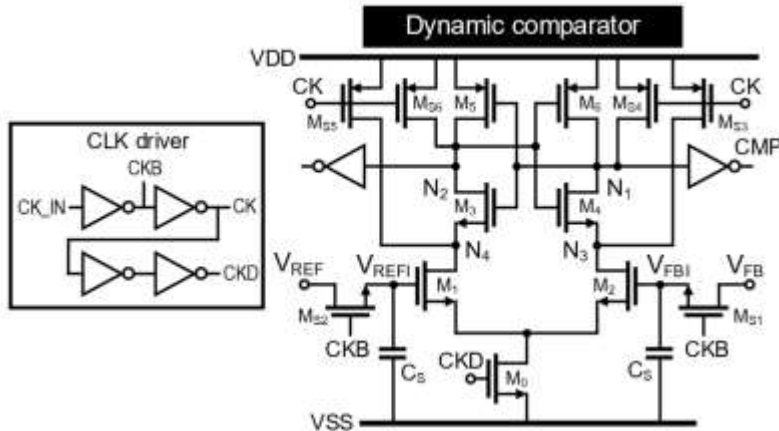


# 1. 저전력 IoT 용 PFM buck converter

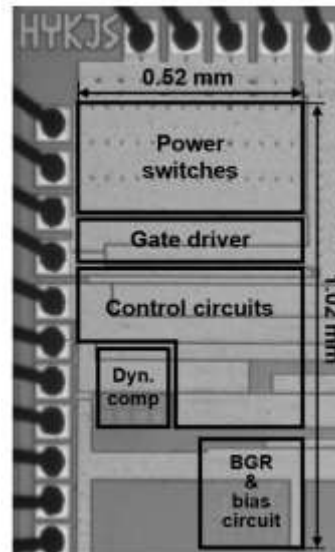
- A High-Light-Load-Efficiency, Low-Ripple-Voltage PFM Buck Converter for IoT Applications
- IEEE Transactions on Power Electronics (IF: 5.967) 2022

고효율 및 저리플 특성을 동시에 갖는 **PFM buck converter** 개발

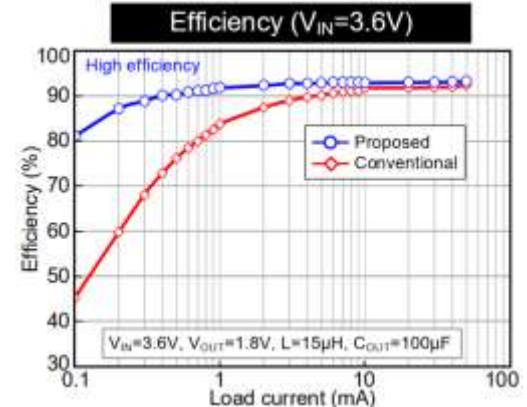
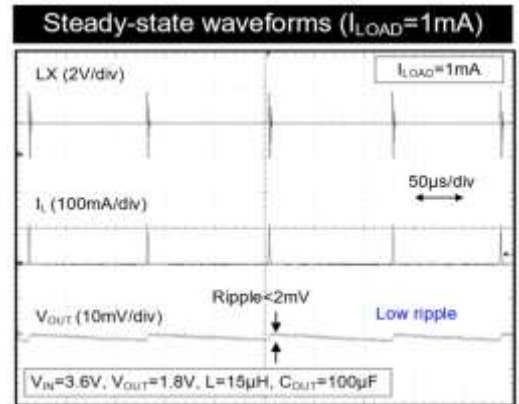
Dynamic comparator → No shoot-through current



\*Process: 350nm CMOS



High efficiency & low ripple



# 1. 저전력 IoT 용 PFM buck converter

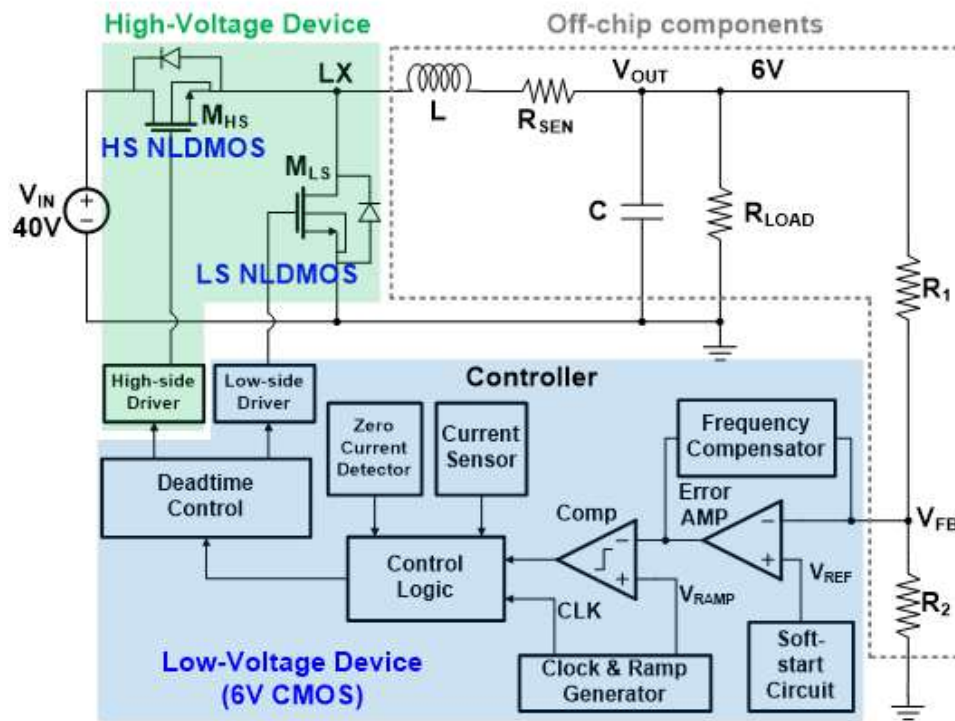
TABLE I  
PERFORMANCE COMPARISON

	[17] LTC 3620	[33] JSSC 2011	[22] TPE 2016	[5] TPE 2017	[34] TCAS-I 2020	[35] TCAS-I 2021	This work				
							with static comparator <sup>1)</sup>	with static comparator <sup>1)</sup>	(proposed) with dynamic comparator	(proposed) with dynamic comparator	
							small C <sub>OUT</sub>	large C <sub>OUT</sub>	large C <sub>OUT</sub>		
Technology	-	45 nm	90 nm	0.13 μm	0.13 μm	0.18 μm	0.35 μm		0.35 μm		
Light-load control method	PFM	PFM	PFM	RM <sup>2)</sup> +PFM	MSPWM <sup>3)</sup> +PFM	DGM <sup>4)</sup> +PFM	PFM		PFM		
Input voltage (V)	2.9–5.5	2.8–4.2	1.8–4.2	2.2–3.3	2.0–3.3	2.7–4.7	2.7–4.2		2.7–4.2		
Output voltage (V)	1.1–2.5	0.4–1.2	0.9–1.4	1.7	1.2	1.6	1.2–1.8		1.2–1.8		
Max. load current (mA)	15	15 (with only light-load controller)	40	10 (with only light-load controller)	15 (with only light-load controller)	20 (with only light-load controller)	50		50	100	
Inductor (μH)	22	10	10	3	1	4.7	15		15	10	
Output capacitor (μF)	1	2	10	3	2.2	4.7	5	100	100	250	
Max. ripple voltage (mV)	19	24	20	>50	15	40	36	3	3	3	
Ripple voltage variation (mV)	15	-	15	-	-	-	33	2	2	2	
Efficiency measurement point	V <sub>IN</sub> =3.0 V V <sub>OUT</sub> =1.8 V	V <sub>IN</sub> =2.8 V V <sub>OUT</sub> =1.0 V	V <sub>IN</sub> =3.3 V V <sub>OUT</sub> =1.2 V	V <sub>IN</sub> =N/A V <sub>OUT</sub> =1.7 V	V <sub>IN</sub> =2.0 V V <sub>OUT</sub> =1.2 V	V <sub>IN</sub> =3.6 V V <sub>OUT</sub> =1.6 V	V <sub>IN</sub> =3.6 V V <sub>OUT</sub> =1.8 V	V <sub>IN</sub> =3.6 V V <sub>OUT</sub> =1.8 V	V <sub>IN</sub> =3.6 V V <sub>OUT</sub> =1.8 V	V <sub>IN</sub> =3.6 V V <sub>OUT</sub> =1.8 V	V <sub>IN</sub> =3.6 V V <sub>OUT</sub> =1.8 V
Efficiency	I <sub>LOAD</sub> =0.1 mA	59%	-	78%	71.5%	48%	78%	75.3%	45.3%	81.1%	80.6%
	I <sub>LOAD</sub> =1 mA	90%	83%	83.5%	82.7%	77%	79%	90.4%	83.8%	91.9%	91.5%
	I <sub>LOAD</sub> =10 mA	93%	87%	87%	90.4%	85%	86%	92.4%	91.8%	93.0%	92.8%
	I <sub>LOAD</sub> =50 mA	-	-	85.6% (@I <sub>LOAD</sub> =40 mA)	-	-	-	92.8%	92.5%	93.4%	93.1%
	I <sub>LOAD</sub> =100 mA	-	-	-	-	-	-	-	-	-	92.8%

- 1) PFM buck converter using a static comparator is fabricated with the same technology used for this article.
- 2) Retention mode (RM).
- 3) Multiple-sawtooth PWM (MSPWM).
- 4) Deep-green mode (DGM).

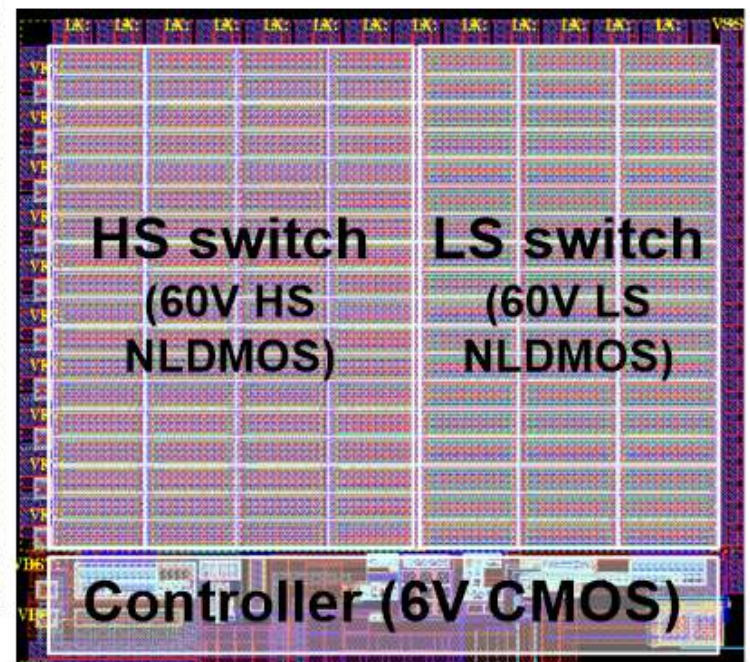
# 2. Automotive Buck-Boost Converter

- Purpose of the circuit
  - To find the effect of parasitic devices between HV & LV devices



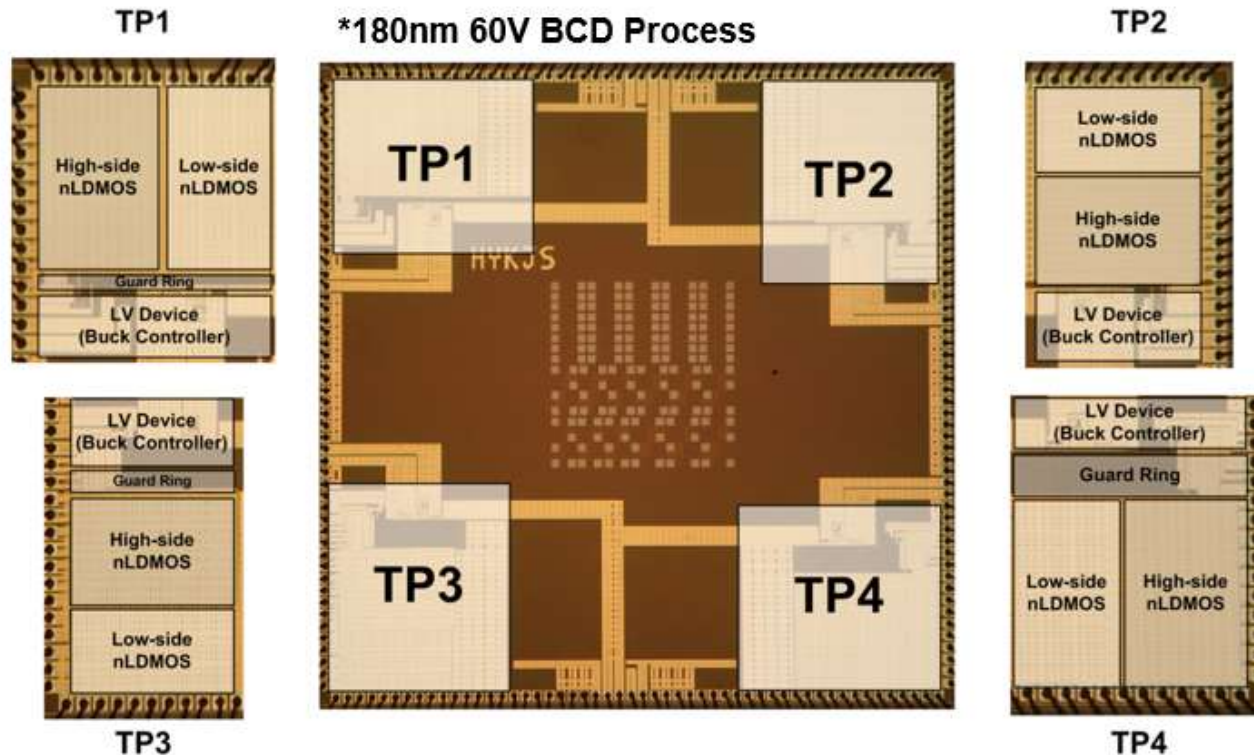
Block diagram

\*180nm 60V BCD Process



Layout

# 2. Automotive $\text{HBM}$ Buck-Boost Converter



TP	Guard-Ring (Width)	Placement of Switches
1	O (15 $\mu\text{m}$ )	Lateral
2	X	Vertical
3	O (200 $\mu\text{m}$ )	Vertical
4	O (200 $\mu\text{m}$ )	Lateral

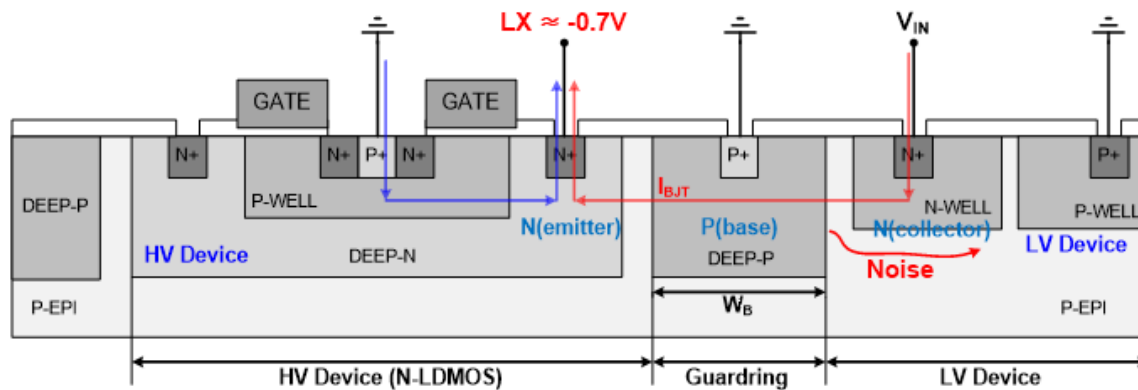
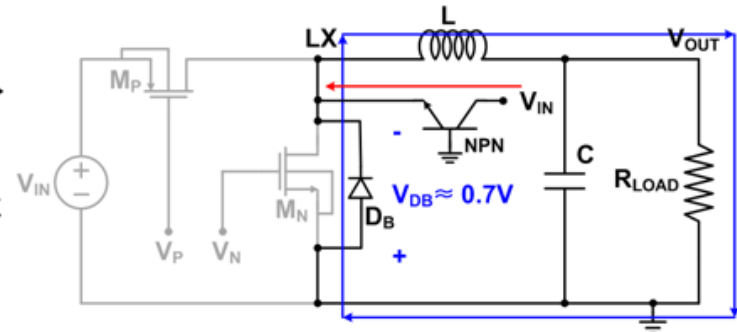
# 2. Automotive Buck-Boost Converter

## ● Operation

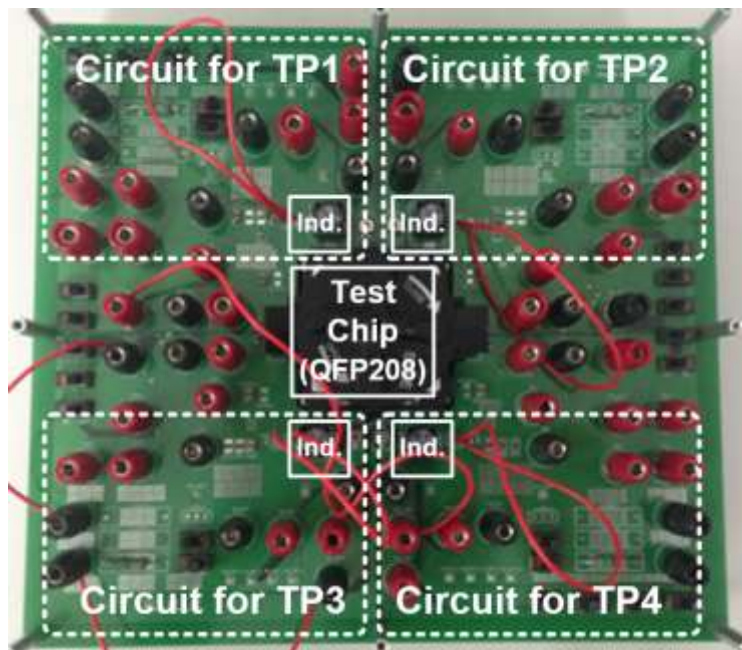
- Dead-time  $\rightarrow$  body diode ON  $\rightarrow$   
 $V_{LX} < -0.7V \rightarrow$  parasitic NPN on  $\rightarrow$   
 substrate noise in LV device region  $\rightarrow$   
 mal-function of DCDC

## ● To reduce the effect of parasitic device

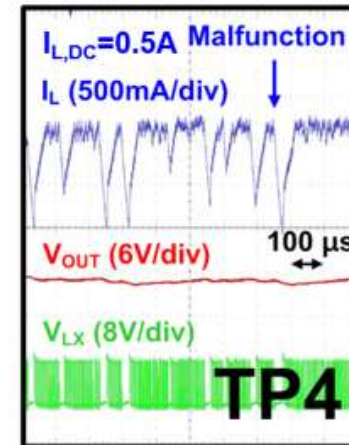
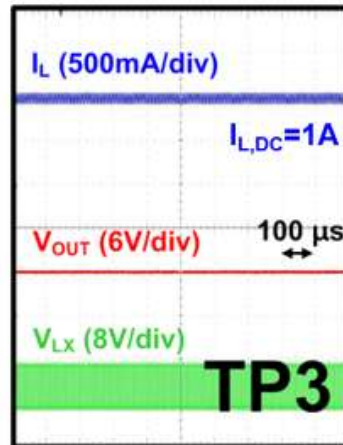
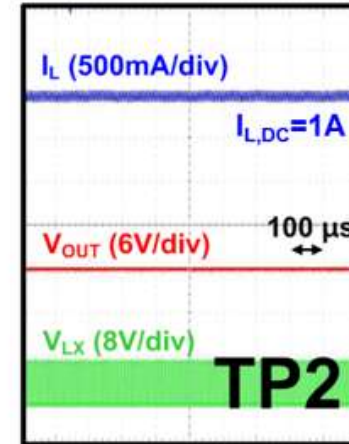
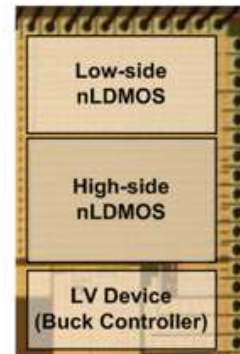
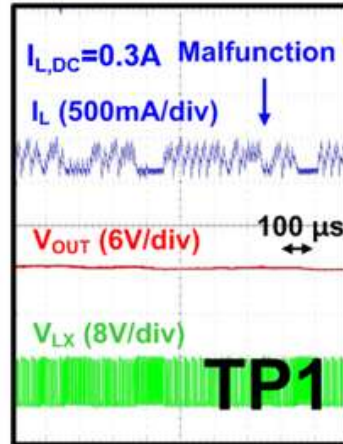
- $\beta$  of NPN should be reduced
  - Large distance between HV and LV



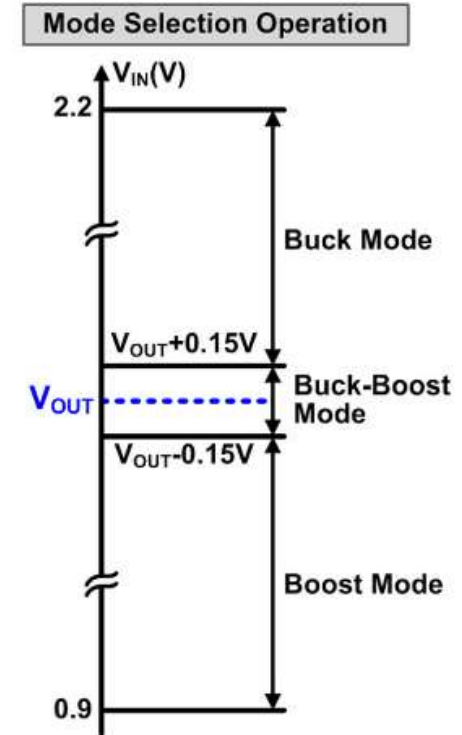
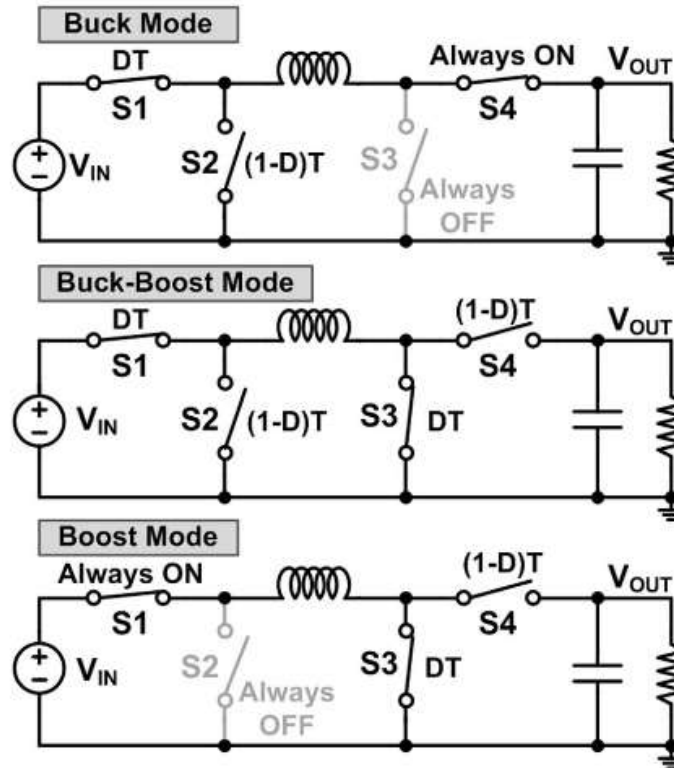
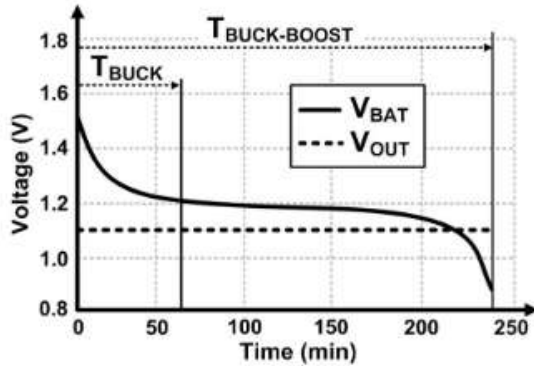
# 2. Automotive 용 Buck-Boost Converter



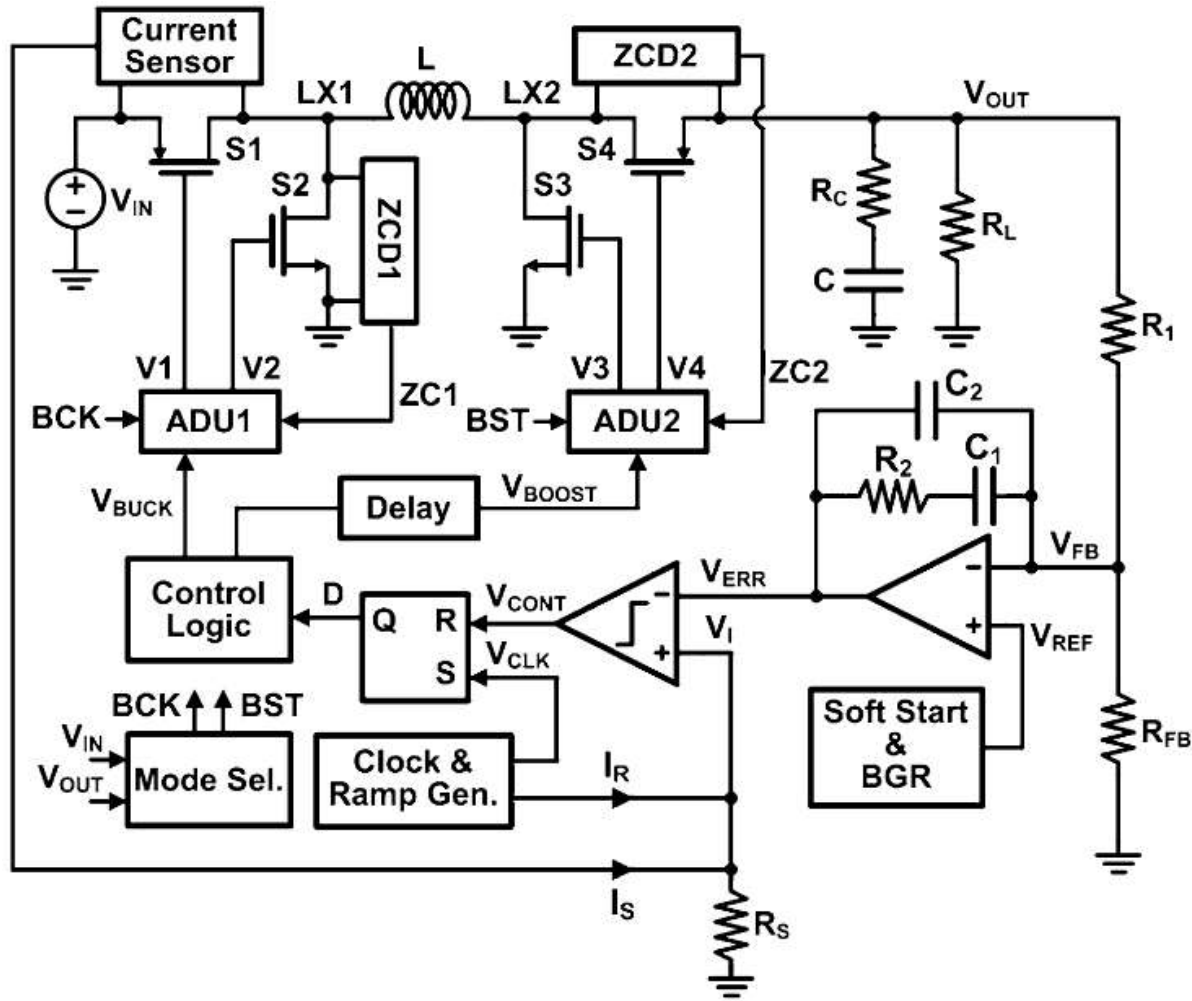
# 2. Automotive Buck-Boost Converter



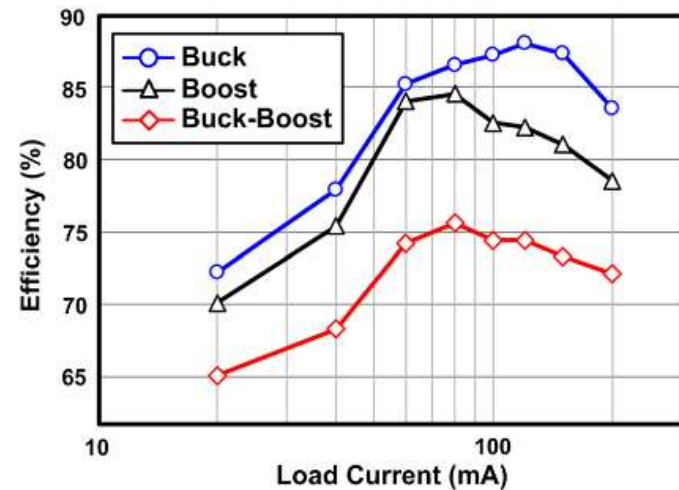
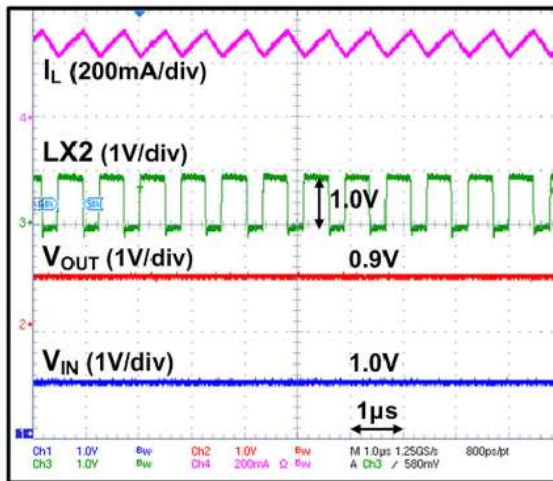
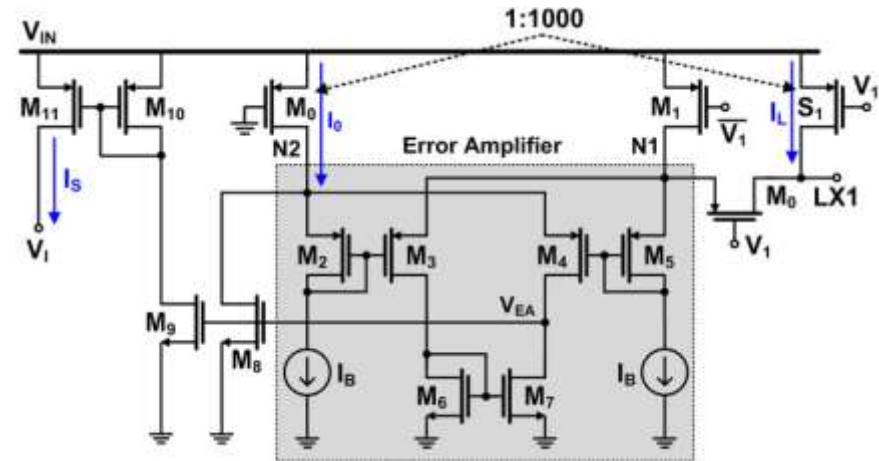
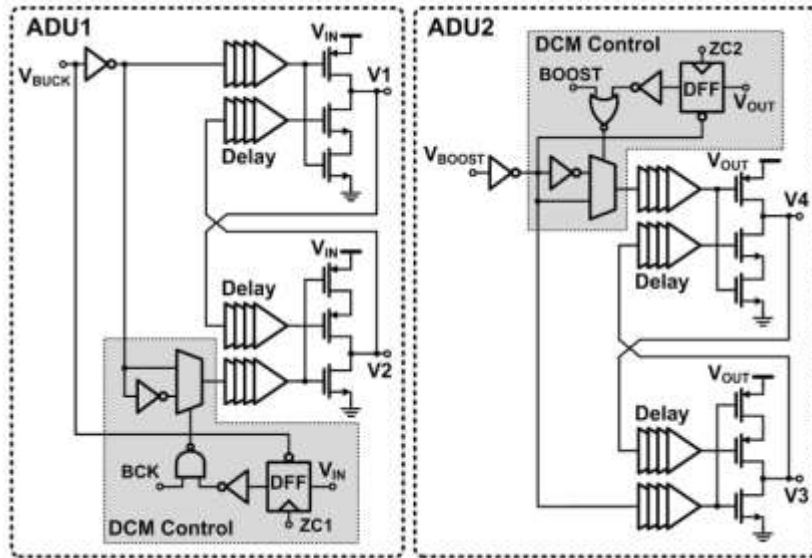
# 3. Mobile용 고효율 buck-boost converter



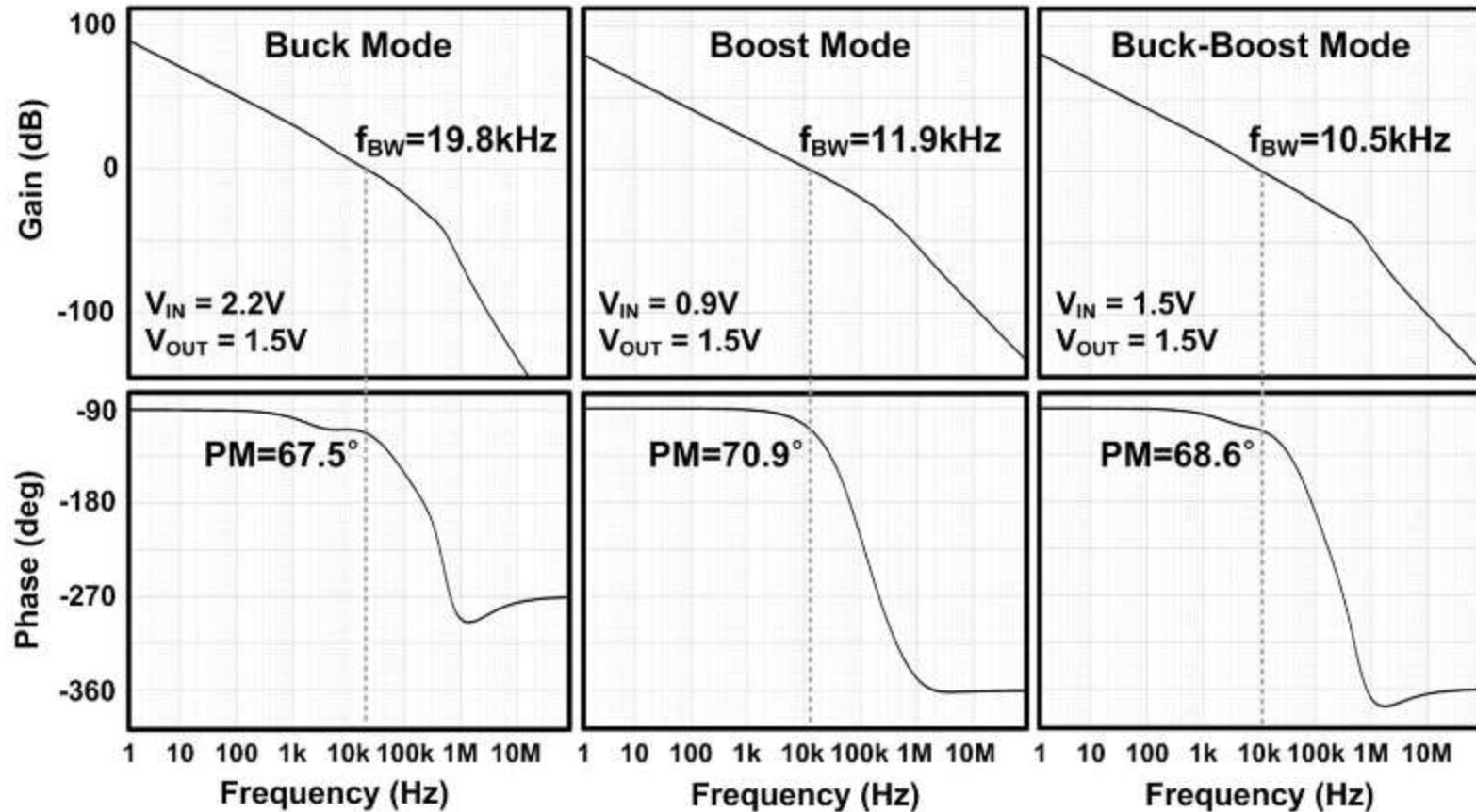
# 3. Mobile용 고효율 buck-boost converter



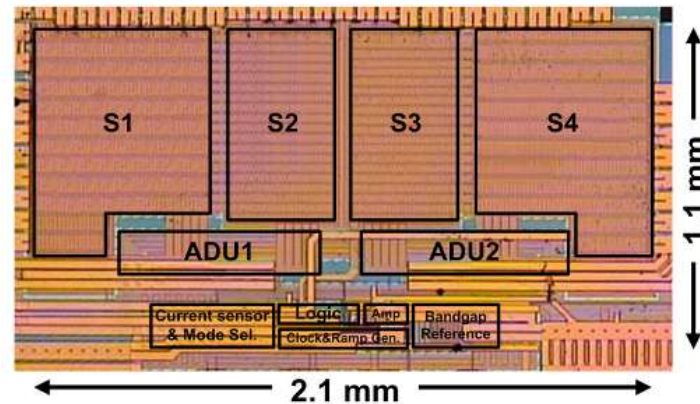
# 3. Mobile용 고효율 buck-boost converter



# 3. Mobile용 고효율 buck-boost converter

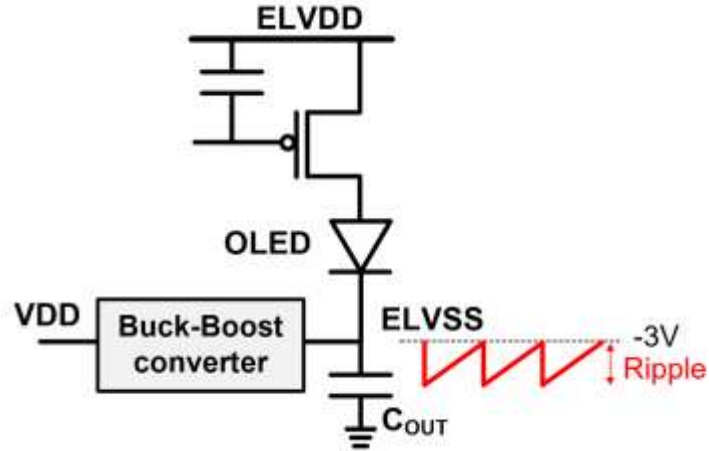


# 3. Mobile용 고효율 buck-boost converter



	[2]	[18]	This work
Process	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	0.18 $\mu\text{m}$
Supply voltage	2.5–5.0 V	2.3–5.0 V	0.9–2.2 V
Inductor	18 $\mu\text{H}$	4.7 $\mu\text{H}$	4.7 $\mu\text{H}$
Capacitor	47 $\mu\text{F}$	22 $\mu\text{F}$	10 $\mu\text{F}$
Switching frequency	0.5 MHz	0.5 MHz	1 MHz
$I_{\text{OUT}}$ (Max)	330 mA	200 mA	200 mA
Output voltage	3.3 V (fixed)	3.3 V (fixed)	0.9–2.2 V (variable)
Max. efficiency (buck mode)	91.6 %	92.0 %	88.0 %
Max. efficiency (boost mode)	<80 %	N/A	84.5 %
Max. efficiency (buck–boost mode)	<65 %	N/A	75.6 %
Line regulation	N/A	0.05 V/V	0.05 V/V

# 4. Buck-Boost Converter for ELVSS

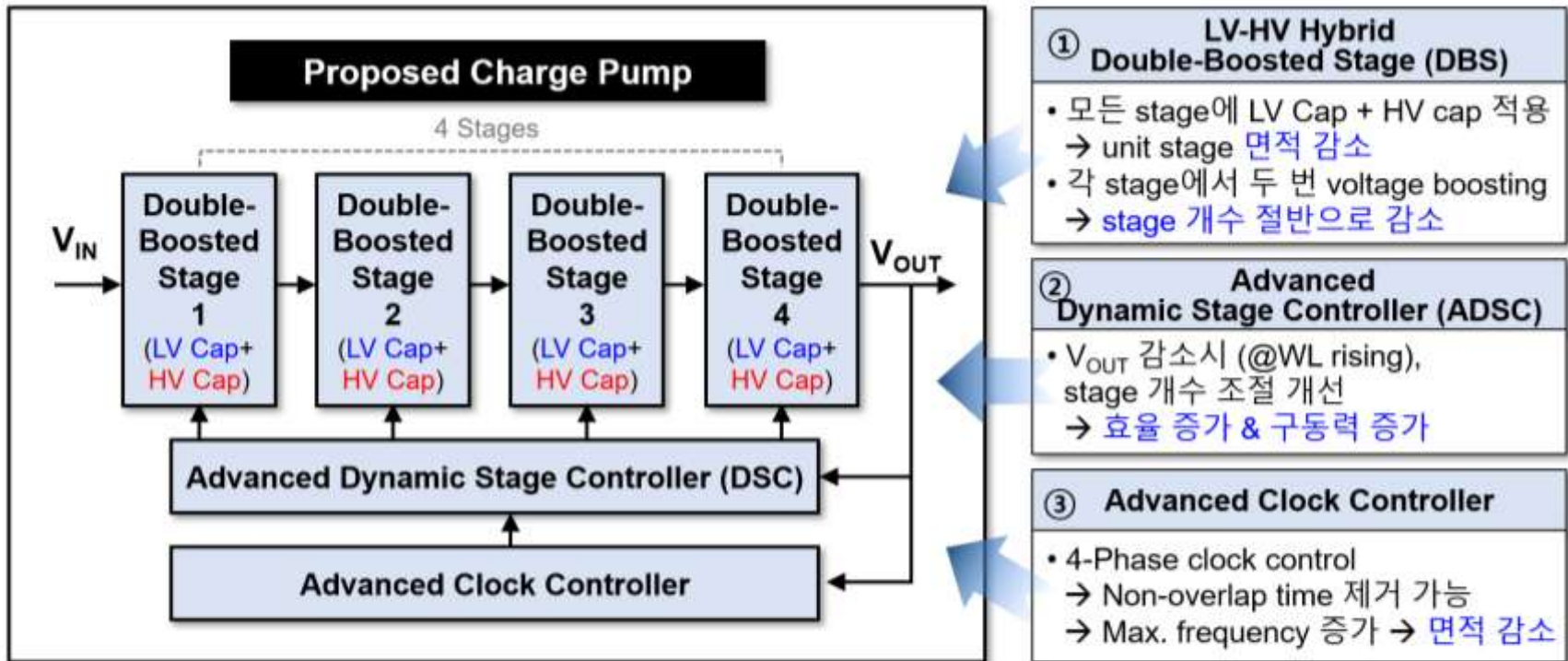


\*연구 진행 중

	Conventional	Typical PFM	Proposed
Control method	PWM (FCCM)	PFM	Advanced PFM
$C_{OUT}$	Large	Large	Large
Ripple	Small (5 mV)	Small (5 mV)	Very small (< 2 mV)
Efficiency at light load (<10mA) *at low gray level	Very bad (reverse current)	Very bad (shoot-through current)	Good

Low ripple, high efficiency 동시 달성 → OLED 화질 향상 & Power 감소 동시 달성

# 5. 4D NAND Flash Memory 용 (320단) 고효율/저면적/고속 Charge Pump (@SK Hynix)



## Advantages

- ① LV-HV Hybrid Double-Boosted Stage → Stage 면적 감소 & Stage 개수 감소
- ② Advanced Dynamic Stage Control (ADSC) → 효율 증가 & 구동력 증가
- ③ Advanced Clock Control → 면적 감소 & 효율 증가

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# [ 연구분야: Biomedical Circuit ]

## 비침습적 뇌자극 회로 및 시스템

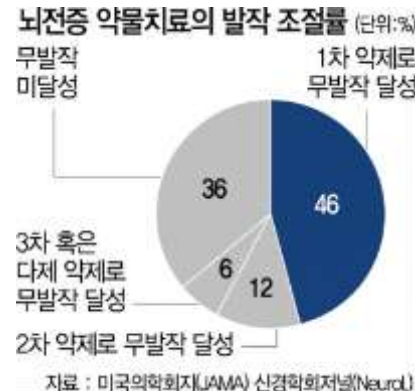
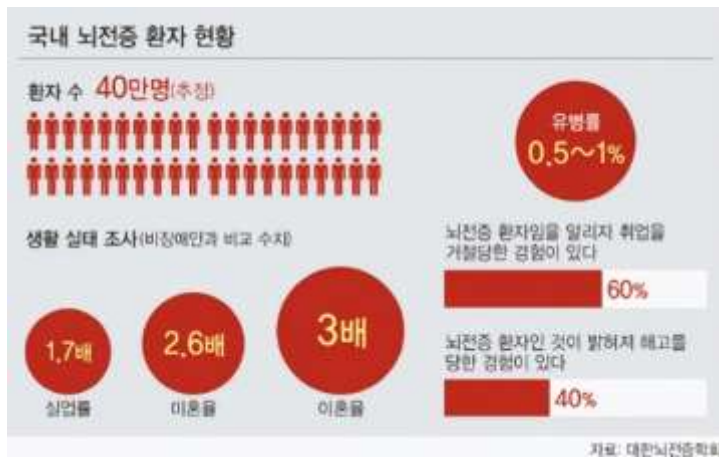
# 뇌전증 치료용 전자약의 필요성

## ● 뇌전증 현황 및 사회경제적 비용

- 뇌전증: 신경의 과도한 흥분으로 비정상 발작이 반복적으로 발생하는 질환
- 인구의 고령화 - 고령층에서 특히 많이 발생하는 뇌전증 케이스의 증가 (국내 뇌전증 환자 약 40만명 추정)
- 급속도로 증가하고 있는 의료적, 복지적, 사회적 비용에 대한 해결책이 필요한 상황

## ● 뇌전증 환자를 위한 현재의 치료법

- 약물치료: 주 치료 방법. 단 약 30%는 약물에 의한 효과가 없는 난치성 뇌전증 환자로 분류
- 수술적 치료: 병변 부위를 대상으로 한 절제 수술. 수술로 인한 뇌기능의 손상 우려



# 기존 전자약 기술의 한계

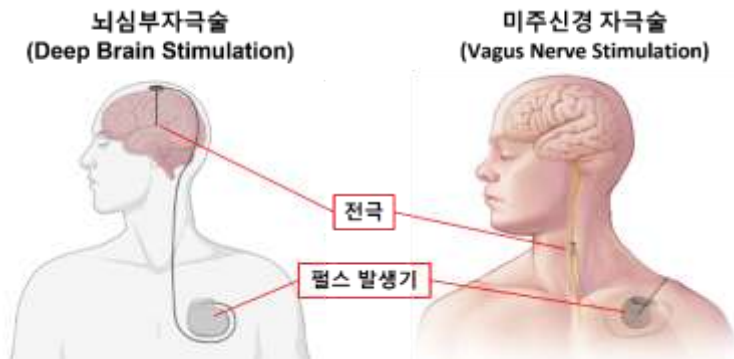
## ● 기존 침습적 전자약 기술의 한계

- 뇌심부자극술(DBS): 뇌에 직접 전극을 임플란트 하여 자극
- 미주신경자극술(VNS): 유연한 형태의 전극을 신경에 감아 자극
  - 매우 높은 난이도의 수술이 요구됨
  - 기기/조직간 물성 차이로 인한 염증 반응: 장기적 사용 제한
  - 타 장기에 의도치 않은 부작용을 초래

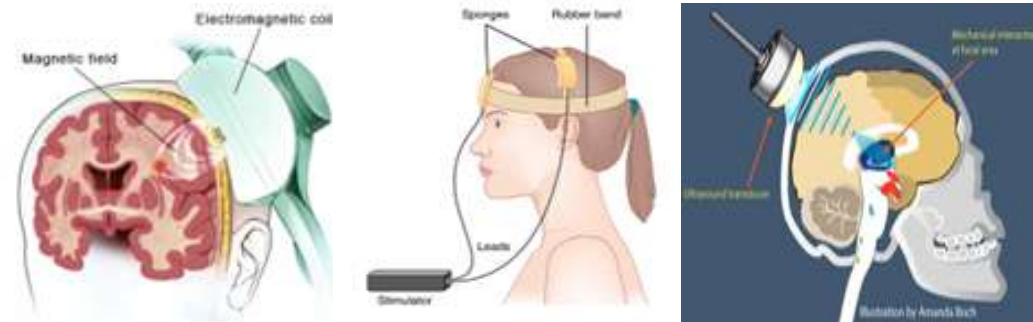
## ● 기존 비침습적 전자약 기술의 한계

- 경두개 직류전기자극법 (tDCS), 경두개 자기 자극법 (TMS), 초음파 신경자극법 (Ultrasonic Modulation)
- 낮은 공간적 해상도: 원하지 않는 부위 자극에 의한 부작용, 깊은 곳에 위치한 신경 자극의 어려움

### 기존 침습적 전자약 기술



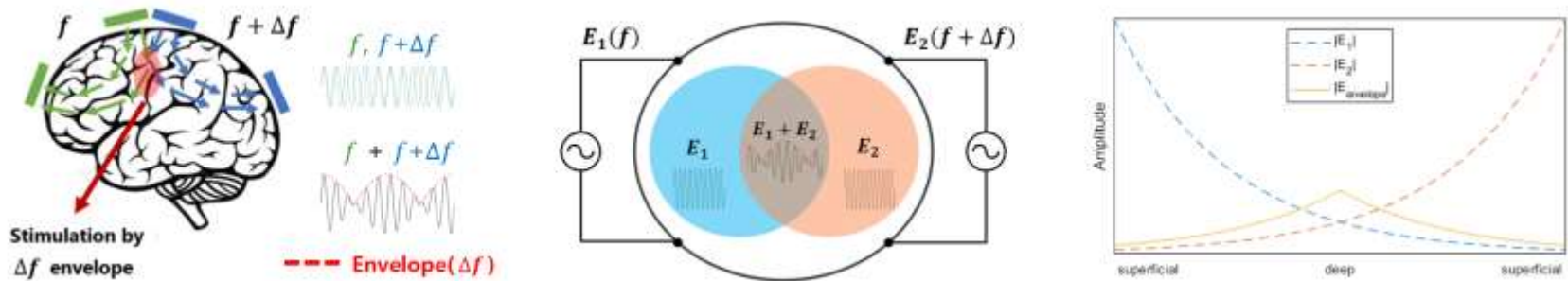
### 기존 비침습적 전자약 기술



# 시간적 간섭 자극술 (Temporal Interference Stimulation, TIS)

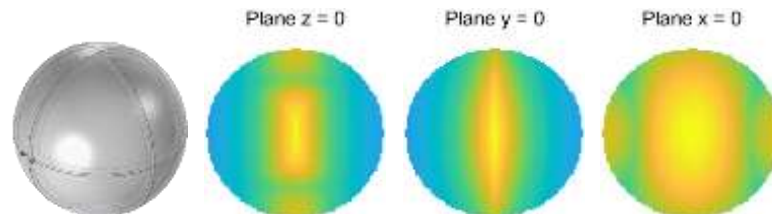
## ● TIS 원리

- 전기장 간의 **간섭으로 인한 맥놀이 현상**을 이용하여 신경을 자극하는 기술
- 신경세포가 고주파에서는 반응하지 않고, 저주파에서는 반응한다는 점을 이용
- 두 고주파 전기장 간섭이 발생한 부분에서만 저주파의 포락선이 형성되어 자극이 이루어짐
- 침습적 방법임에도 불구하고 **뇌심부를 선택적으로 자극할 수 있다는 장점**



## ● TIS 기술의 현재 한계점

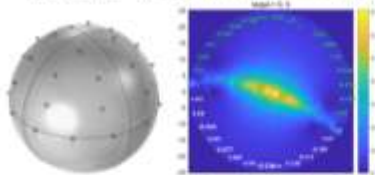
- 침습적 방법에 비해서는 여전히 **공간적 해상도 부족**
- 목표영역 자극을 위한 **전극위치 및 자극강도 선택의 어려움**
- 동시에 **다지점 자극 불가**



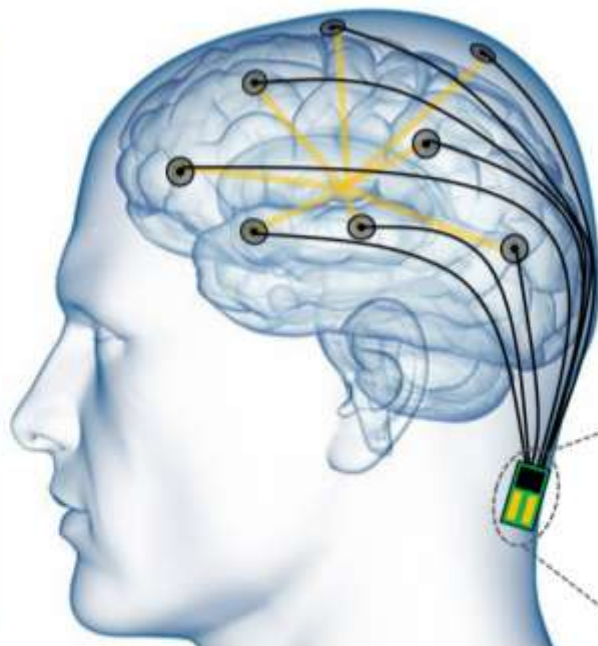
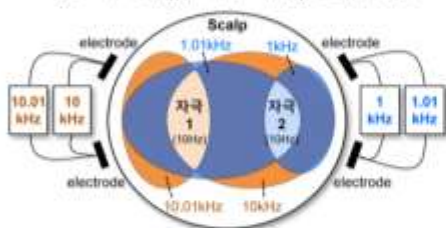
# Multi-TIS 회로 및 시스템 개발

## 핵심기술1. Multi-TIS 효율성 검증 및 측정 시스템 구축

다채널 출력(고정밀 자극) 효과 검증



다중 주파수(다지점 자극) 효과 검증



## 핵심기술2. Multi-TIS IC Chip 설계 기술



Chip 내 회로 집적 → 시스템 소형화  
 다채널 출력 → 고정밀 자극  
 다중 주파수 출력 → 다지점 자극  
 불균일도 보상회로 내장 → 고균일 자극

## 핵심기술3. Multi-TIS 시스템 보드 설계 기술

무선 Multi-TIS 시스템 보드



\*유연한 PCB에 시스템 구현

## 핵심기술1. Multi-TIS 효율성 검증 및 측정 시스템 구축

다채널 출력 (고정밀 자극), 다중 주파수 (다지점 자극) 효과 검증 및 측정 시스템 구축

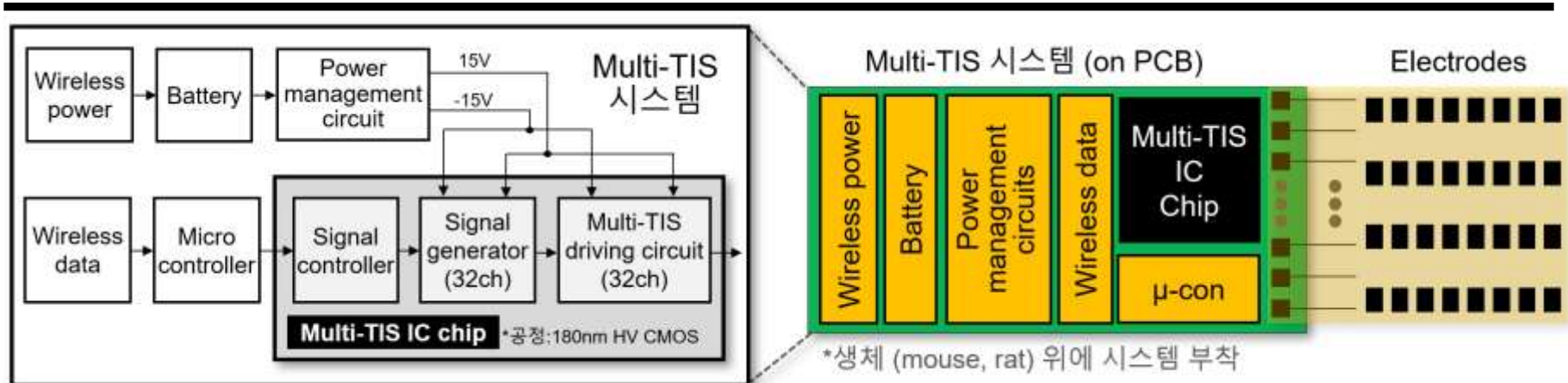
## 핵심기술2. Multi-TIS IC Chip 설계 기술

다채널 (고정밀), 다중 주파수 (다지점), 불균일도 보상 (고균일) 기능을 갖는 회로를 전용 IC chip으로 구현

## 핵심기술3. Multi-TIS 시스템 보드 설계 기술

무선 데이터 전송 및 채널 불균일도 보상 제어 가능한 시스템 보드 개발

# Multi-TIS 회로 및 시스템 개발



## 핵심 개발 기술

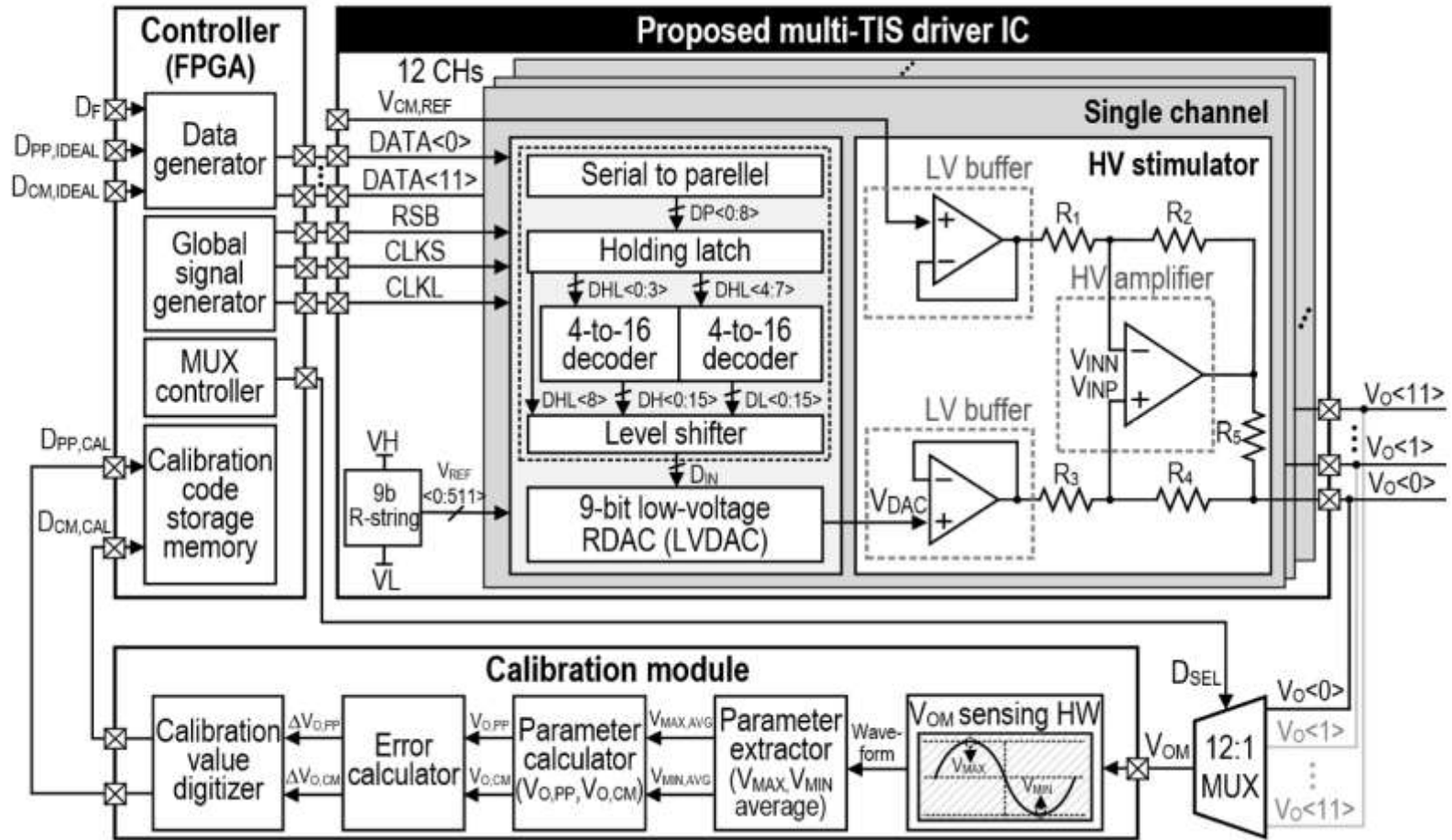
- 고정밀 주파수 생성 회로 (0.1% 단위 주파수 조절 가능)
- 고전압 ( $\pm 15V$ ) 고균일 (mismatch < 0.1%) 구동회로
- 다채널 IC chip (최대 32 ch)
- 무선 데이터 / 전력 전송 회로

## 연구 진행 상황 및 계획

- 2023: 전용 IC chip 구성회로 설계 완료
- 2023: 1차 시제품 (IC chip) 제작 중: TSMC 180nm BCD 공정
- 2024: 2차 시제품 (IC chip) 제작
- 2025: 2차 시제품 (IC chip) 이용한 시스템 구성 및 생체 (rat, mouse) 대상 실험

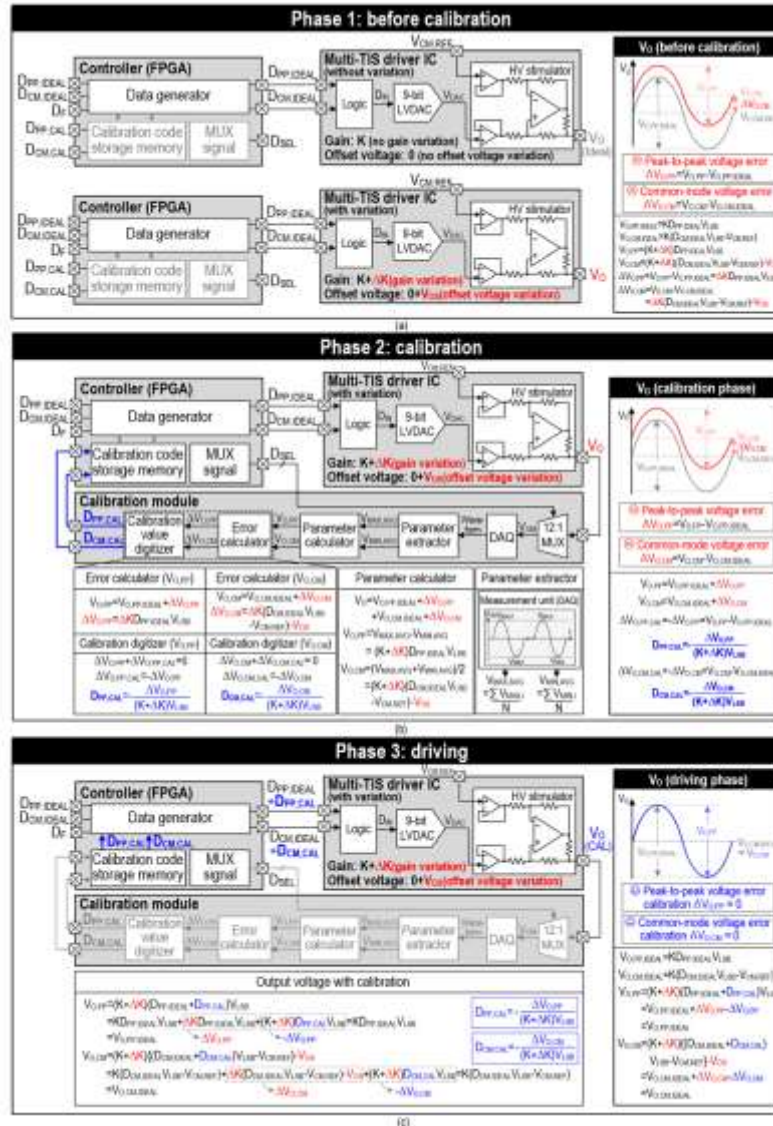


# TIS IC Chip 개발 내용

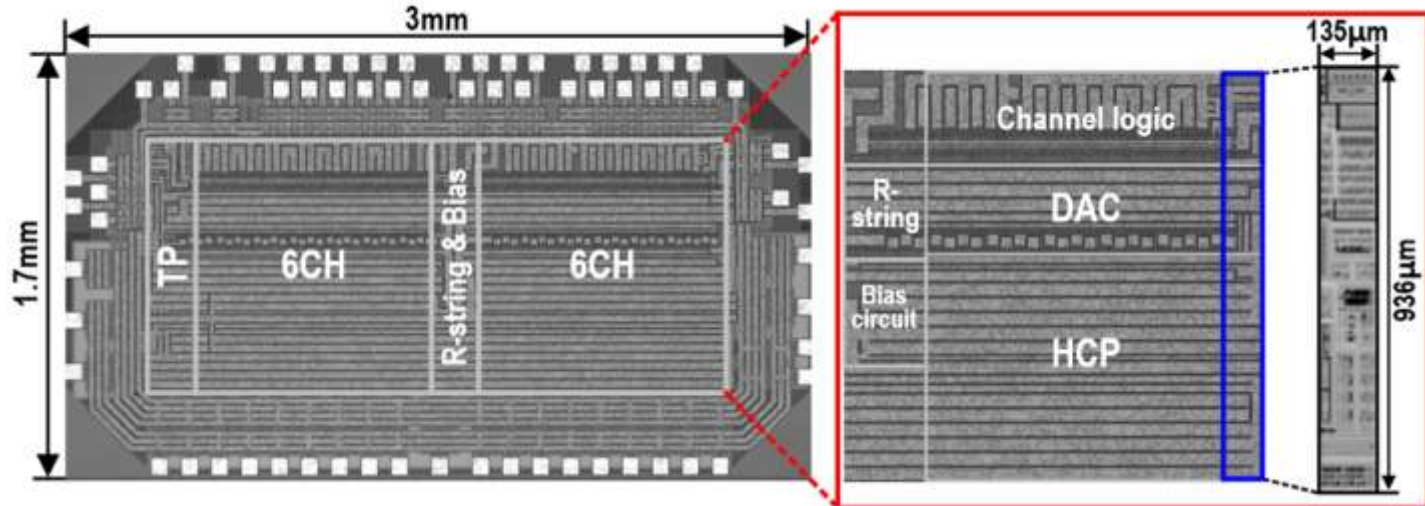




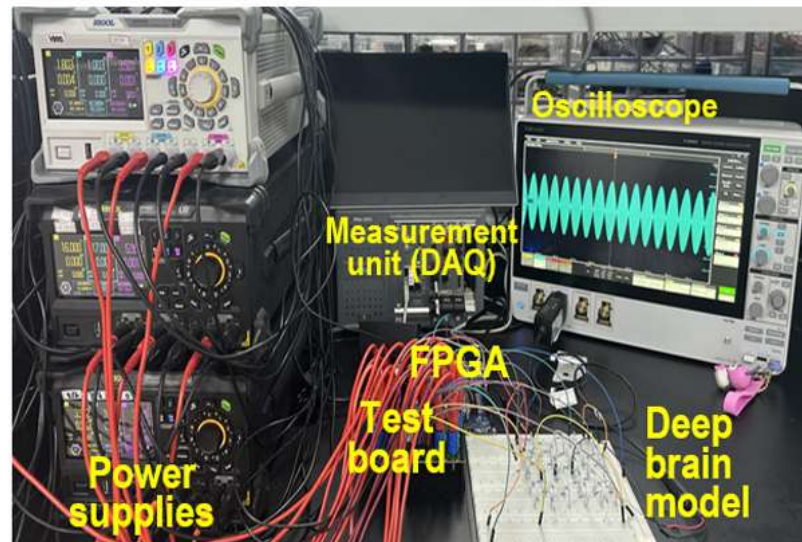
# TIS IC Chip 개발 내용



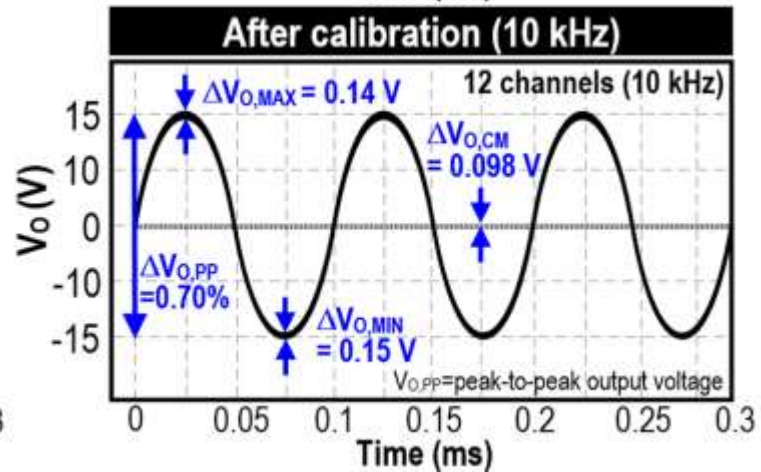
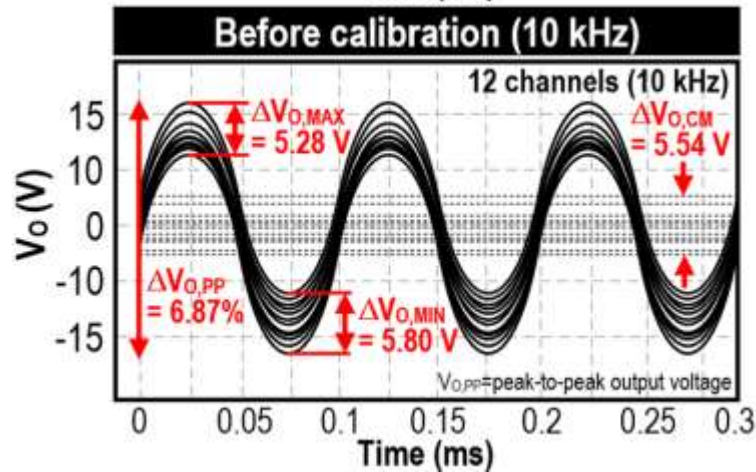
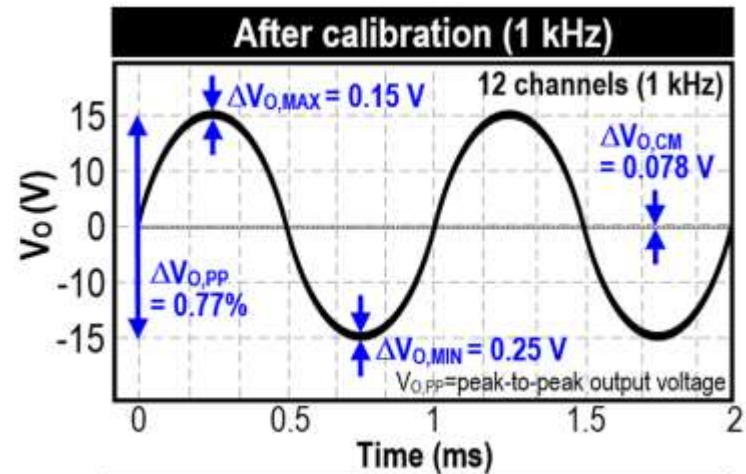
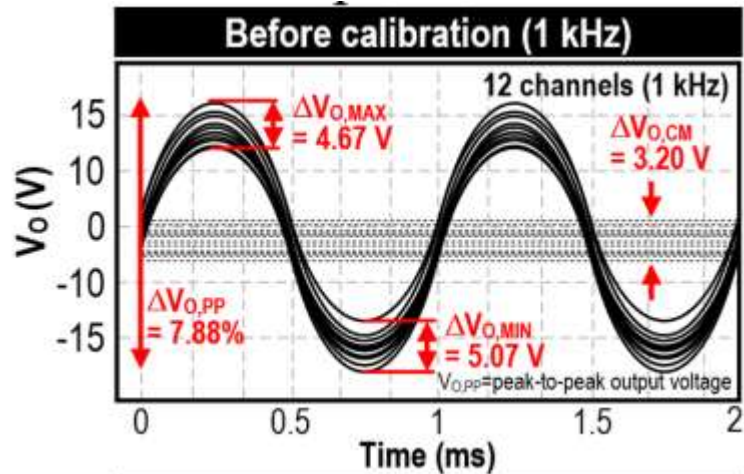
# TIS IC Chip 개발 내용



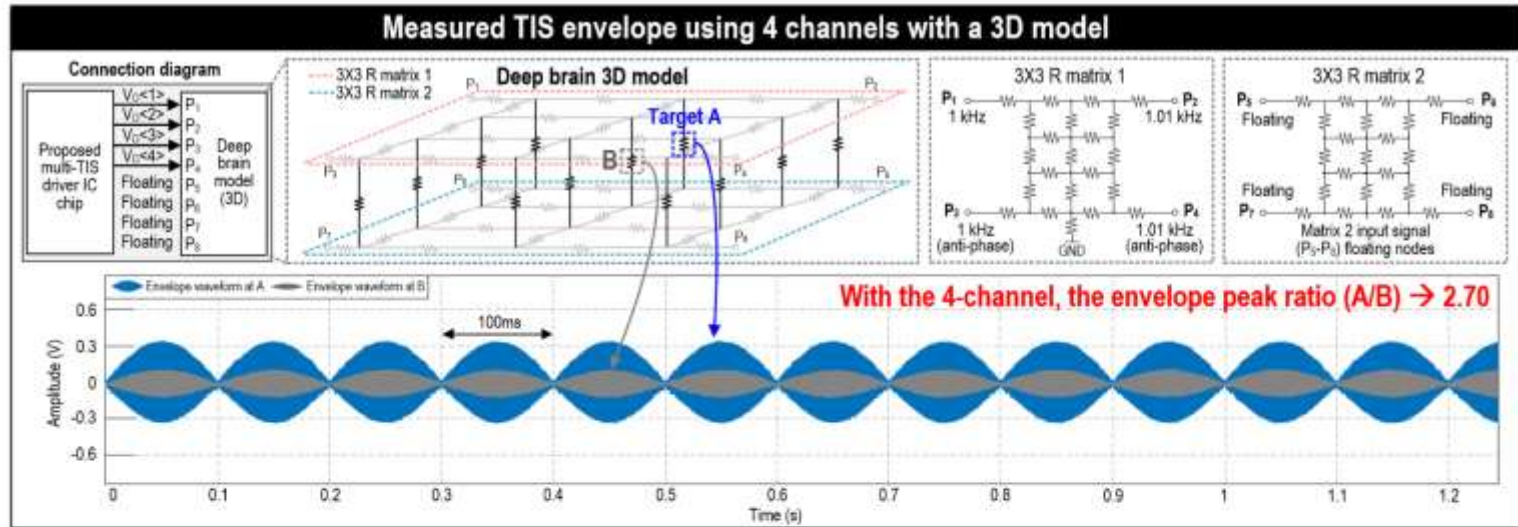
공정: TSMC 180nm BCD



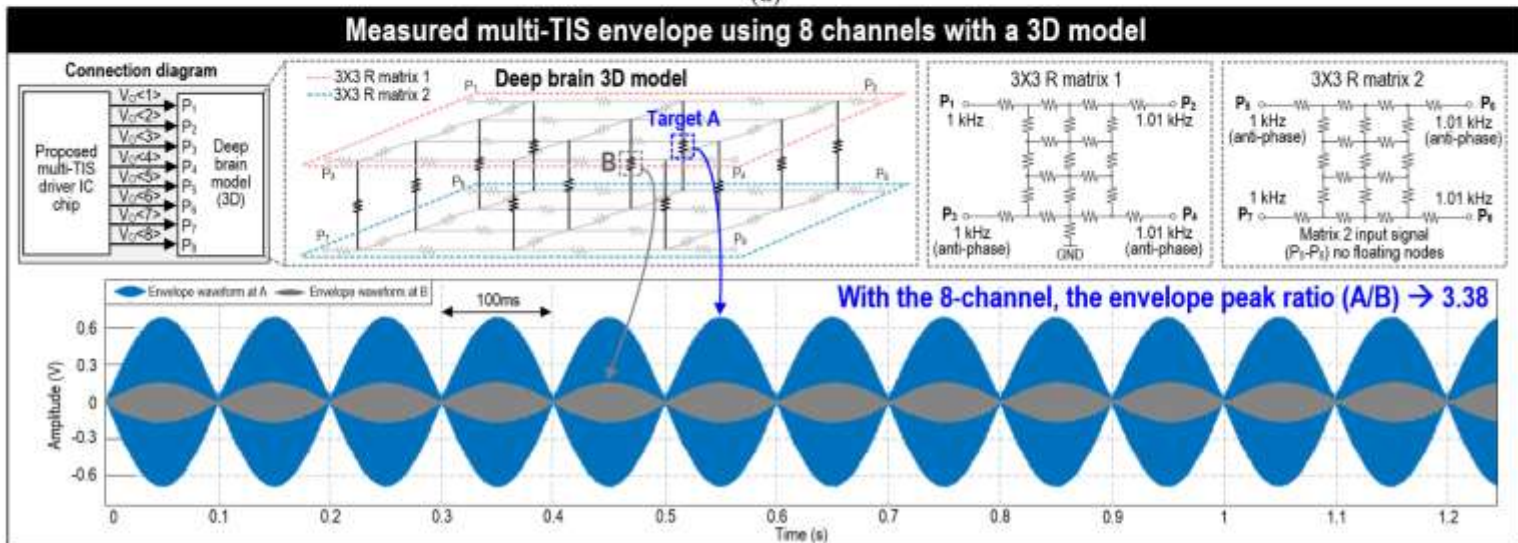
# TIS IC Chip 개발 내용



# TIS IC Chip 개발 내용



(a)



# TIS IC Chip 개발 내용

	[16] CICC 24	[17] TBioCAS 25	[14] JSSC 24	<b>This work</b>
Technology	180nm CMOS	180nm CMOS	130nm BCD	180nm BCD
Application	PNS	PNS	VNS	VNS, Brain stim.
Stimulation method	Bipolar	Tripolar	Single-TIS	<b>Multi-TIS</b>
TIS compatibility	No	No	Yes	<b>Yes</b>
Multi-TIS compatibility	No	No	No	<b>Yes</b>
Stimulation waveform	Bi-phasic	Bi-phasic	Sinusoidal	Sinusoidal
Stimulation current generation scheme	Separated source/sink	Separated source/sink	Separated source/sink	<b>Unified source/sink</b>
Maximum simultaneously driven electrodes	8	6	4	<b>12</b>
Maximum stimulation current (mA)	3.5	0.124	10.22	2
Stimulation current resolution ( $\mu$ A)	N/A	2	20 <sup>a</sup>	7.8
Stimulation current maximum frequency (Hz)	N/A	20k	42k	10k
Stimulation current frequency resolution (Hz)	N/A	N/A	10	10
Compliance voltage (V)	20	45	10	$\pm 20$ V
Maximum load ( $\Omega$ )	N/A	100k	1.8k <sup>b</sup>	15k
Channel area (mm <sup>2</sup> )	0.06	0.64	0.13 (without DAC)	<b>0.13 (with DAC)</b>
DAC resolution	12b	5b	9b	9b
With calibration	No	Yes	Yes	Yes
Deviation of common-mode voltage (after calibration)	N/A	N/A	N/A	$\Delta V_{CM} \leq 98$ mV
Deviation of peak-to-peak voltage (after calibration)	N/A	N/A	N/A	$\Delta V_{PP} \leq 0.77$ %
Maximum SFDR (dB)	N/A	N/A	< 60 <sup>c</sup>	<b>65</b>
Maximum SNDR (dB)	N/A	N/A	< 52 <sup>c</sup>	<b>61</b>
Minimum THD (%)	N/A	N/A	N/A	<b>0.084%</b> <sup>d</sup>

<sup>a</sup> The output current resolution is calculated based on output current 10.22mA.

<sup>c</sup> The SFDR and SNDR were estimated from the accompanying graph.

<sup>b</sup> Stimulation current amplitude of 2.56mA.

<sup>d</sup> THD was calculated considering up to the 9th harmonic component.

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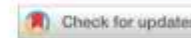
# [Biomedical Circuit]

## 인공피부 시스템 개발

# Reference

This presentation is based on the following paper.

“An artificial neural tactile sensing system,” *Nature Electronics*, Vol. 4, No.6, June, 2021



## An artificial neural tactile sensing system

**Co-first author**

Sungwoo Chun<sup>1,2,3,14</sup>✉, Jong-Seok Kim<sup>4,14</sup>, Yongsang Yoo<sup>4</sup>, Youngin Choi<sup>5</sup>, Sung Jun Jung<sup>5</sup>, Dongpyo Jang<sup>6</sup>, Gwangyeob Lee<sup>7</sup>, Kang-Il Song<sup>8</sup>, Kum Seok Nam<sup>9</sup>, Inchan Youn<sup>8</sup>, Donghee Son<sup>8,10</sup>, Changhyun Pang<sup>1,2</sup>, Yong Jeong<sup>9,11</sup>, Hachul Jung<sup>12</sup>, Young-Jin Kim<sup>12</sup>, Byong-Deok Choi<sup>4</sup>, Jaehun Kim<sup>13</sup>, Sung-Phil Kim<sup>13</sup>, Wanjun Park<sup>4</sup> and Seongjun Park<sup>9,11</sup>✉

Humans detect tactile stimuli through a combination of pressure and vibration signals using different types of cutaneous receptor. The development of artificial tactile perception systems is of interest in the development of robotics and prosthetics, and artificial receptors, nerves and skin have been created. However, constructing systems with human-like capabilities remains challenging. Here, we report an artificial neural tactile skin system that mimics the human tactile recognition process using particle-based polymer composite sensors and a signal-converting system. The sensors respond to pressure and vibration selectively, similarly to slow adaptive and fast adaptive mechanoreceptors in human skin, and can generate sensory neuron-like output signal patterns. We show in an ex vivo test that undistorted transmission of the output signals through an afferent tactile mouse nerve fibre is possible, and in an in vivo test that the signals can stimulate a rat motor nerve to induce the contraction of a hindlimb muscle. We use our tactile sensing system to develop an artificial finger that can learn to classify fine and complex textures by integrating the sensor signals with a deep learning technique. The approach can also be used to predict unknown textures on the basis of the trained model.

\*공동연구(주저자):

고려대 천성우 교수(sensor), 한양대 김종석 교수(circuit & system), 서울대 박성준 교수(biology)

# Future Applications of Artificial Skin

## Prosthetics



## Remote Robot



## Artificial Surgery



## Entertainment



Image courtesy: KIST

# Artificial Skin

Compared to other senses,  
tactile requires more research and development.

## Sense of Vision

Commercial Product  
“Artificial Retina”

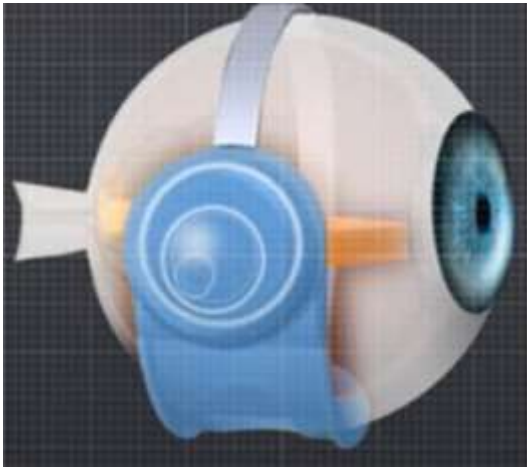


Image courtesy: Second Sight

## Sense of Hearing

Commercial Product  
“Artificial Cochlear”



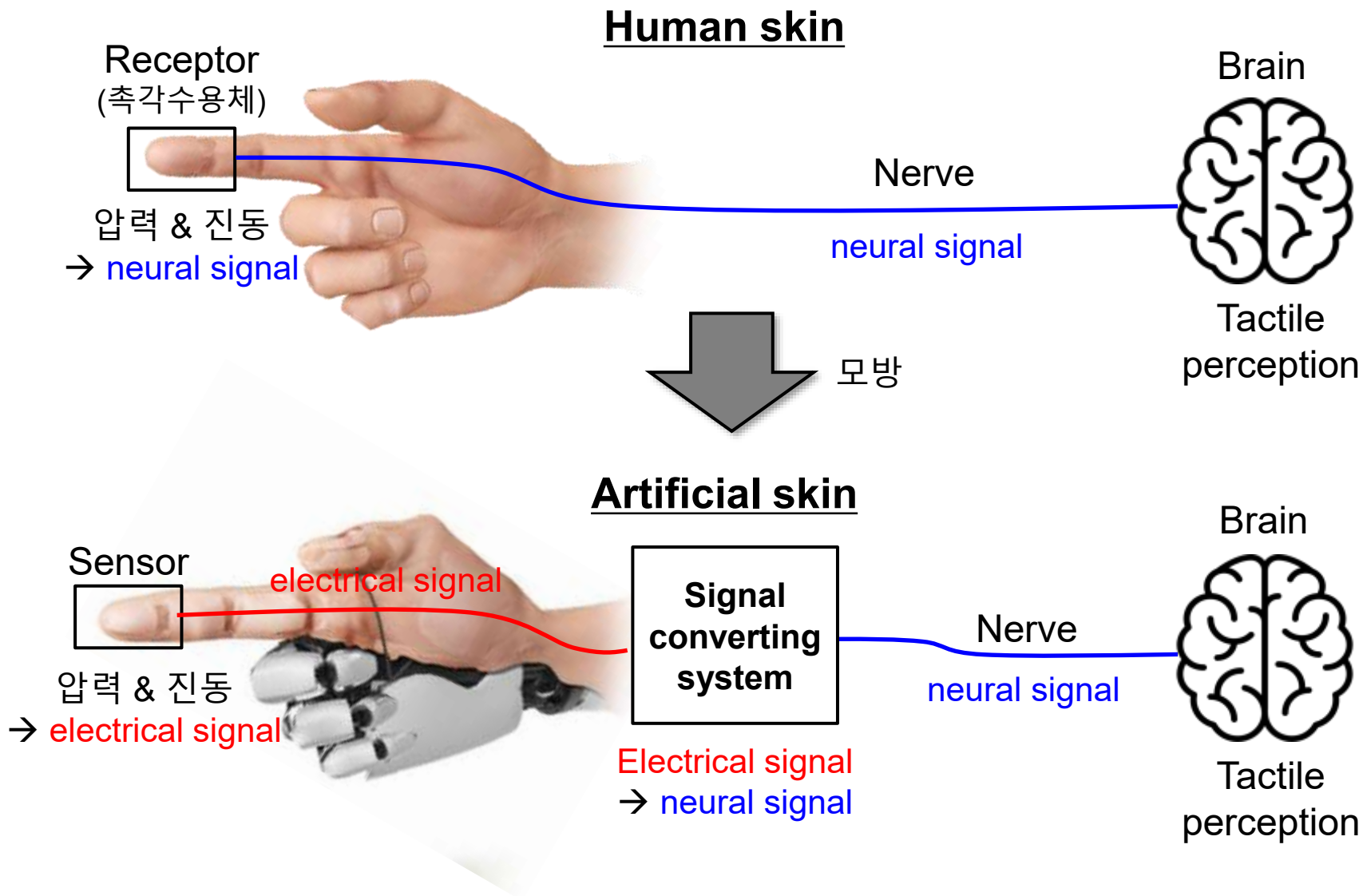
Image courtesy: Medical Device Network

## Sense of Tactile

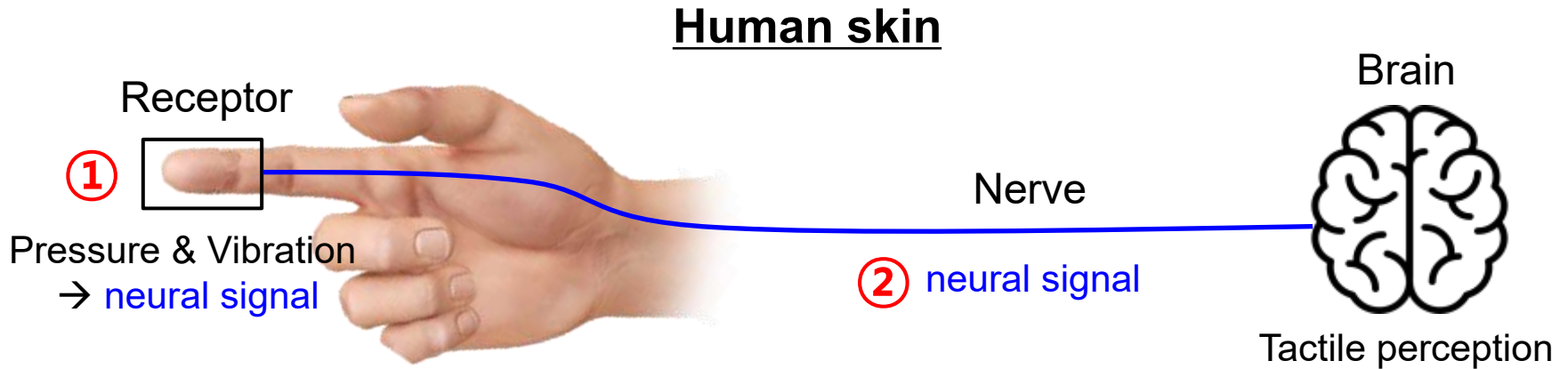
Commercial Product  
“Artificial Skin”

No  
commercial product

# Human Skin VS. Artificial Skin

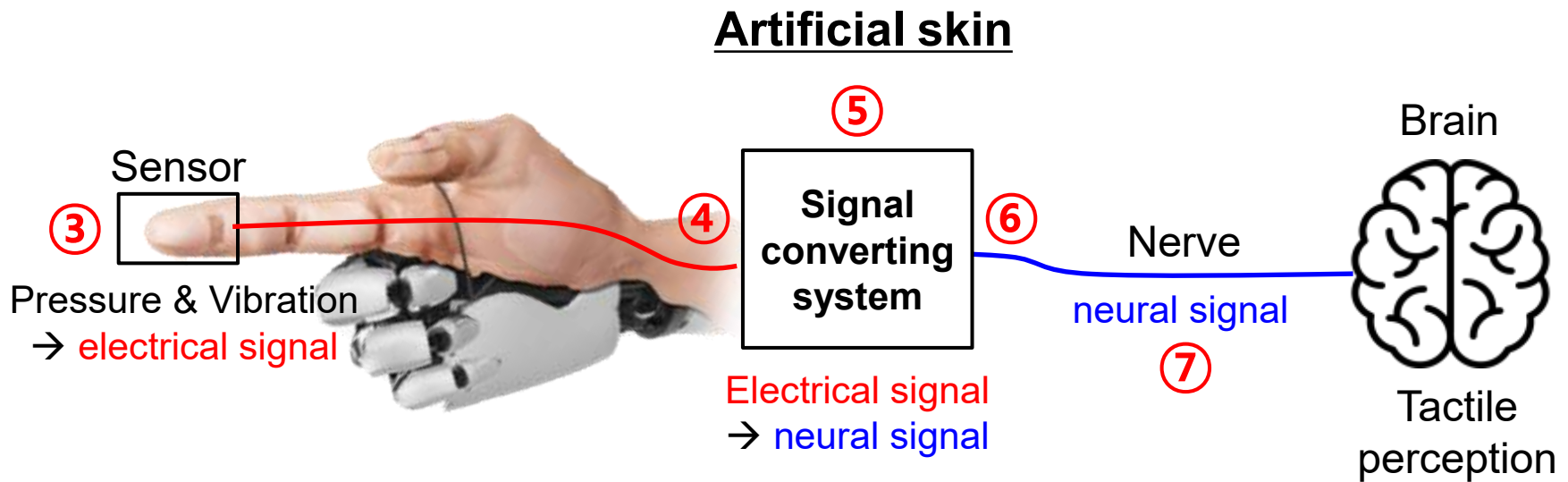


# Research Items



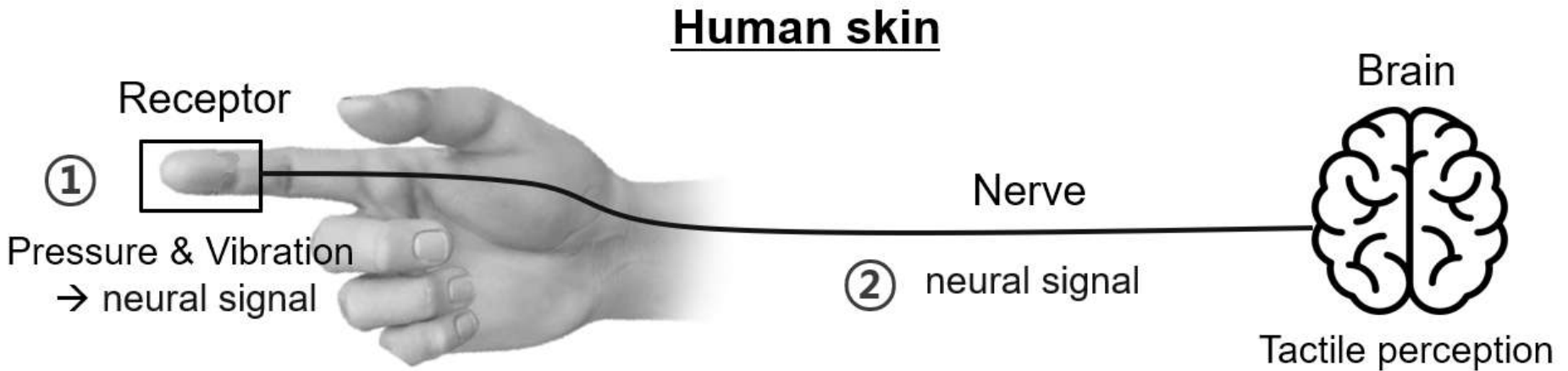
- ① 촉각수용체(receptor)의 종류?
- ② 촉각수용체(receptor)에서 생성되는 neural signal 의 형태?

# Research Items



- ③ **센서**: 인간 촉각수용체(receptor) 를 어떻게 모방할 수 있나?
- ④ **센서 readout**: 센서 전기 신호를 왜곡 없이 읽는 방법?
- ⑤ **Signal converting**: 센서에 인가된 물리적 정보를 판단하고, neural signal을 생성
- ⑥ **Neural stimulator**: 신경이 인식할 수 있는 형태로 신호 변경 및 신경 구동
- ⑦ **생체실험**: 신경에서 신호가 잘 전달됨을 확인하는 방법?

# Research Items



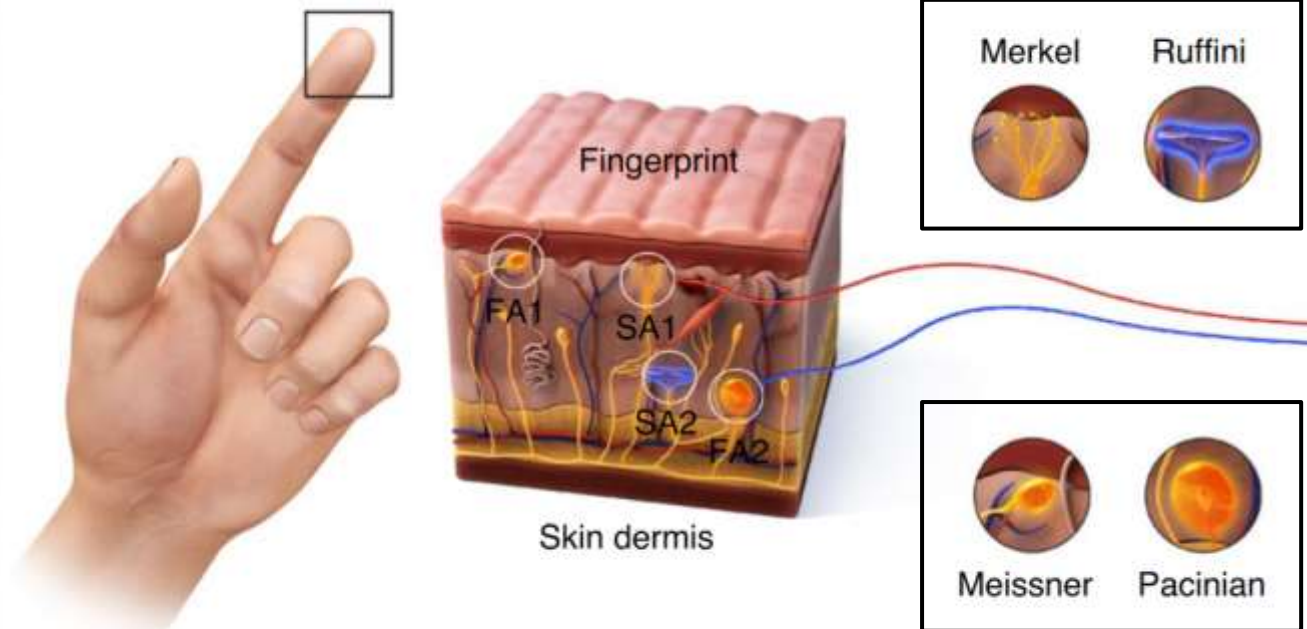
- ① 촉각수용체(receptor)의 종류?
- ② 촉각수용체(receptor)에서 생성되는 neural signal 의 형태?

# Biological Tactile Sensory System

## ● Human Tactile Perception

- Human perceives tactile stimuli through the mechanoreceptors.
- **Slow adaptive (SA)** receptors respond to the static **pressure**
- **Fast adaptive (FA)** receptors respond to the **vibration** (high-frequency dynamic pressure)

Biological tactile sensory system



**SA receptors:**  
respond to static **pressure**



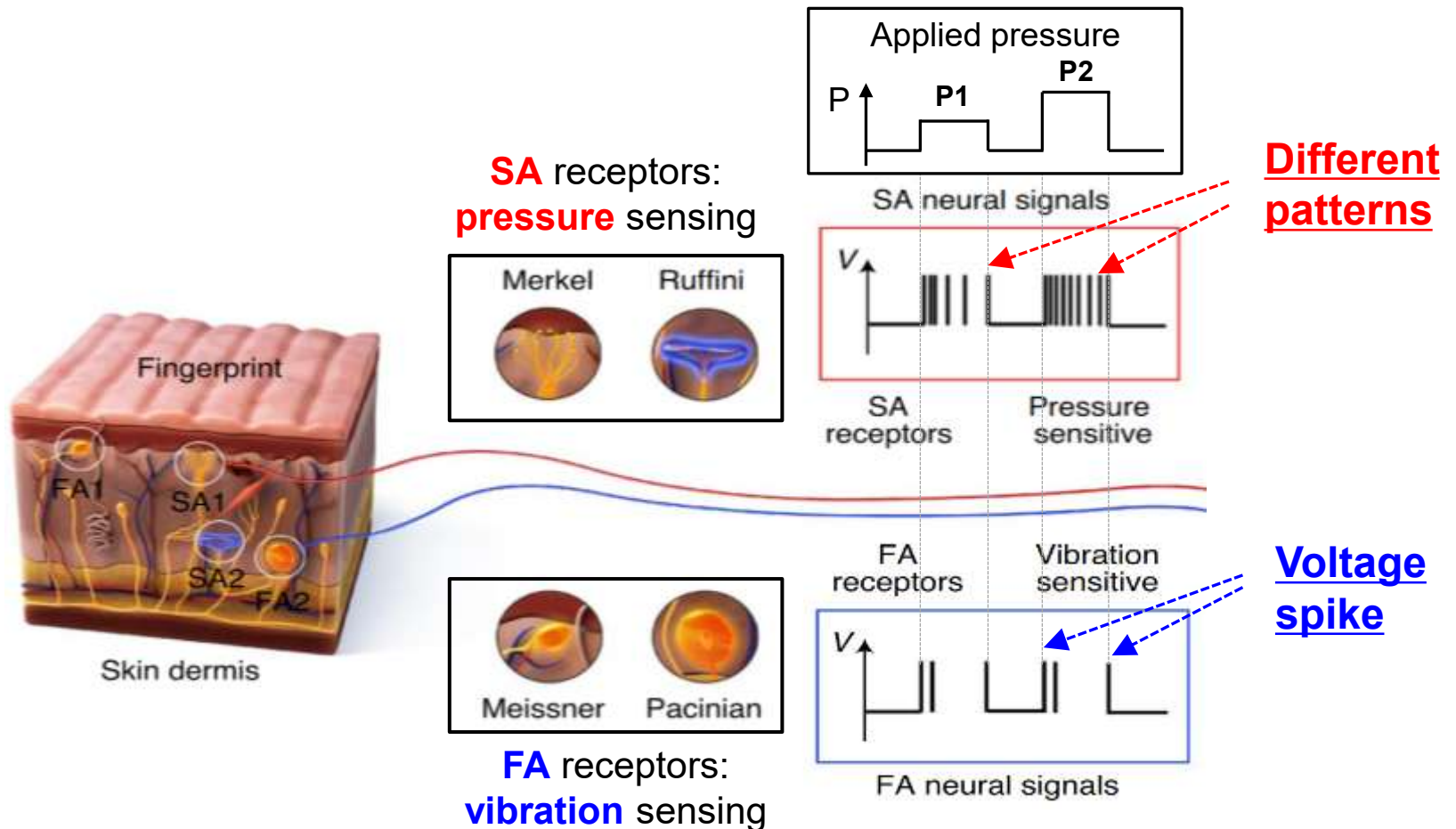
**FA receptors:**  
respond to **vibration**

\*vibration: high-frequency dynamic pressure

# Biological Tactile Sensory System

## ● Neural Signals

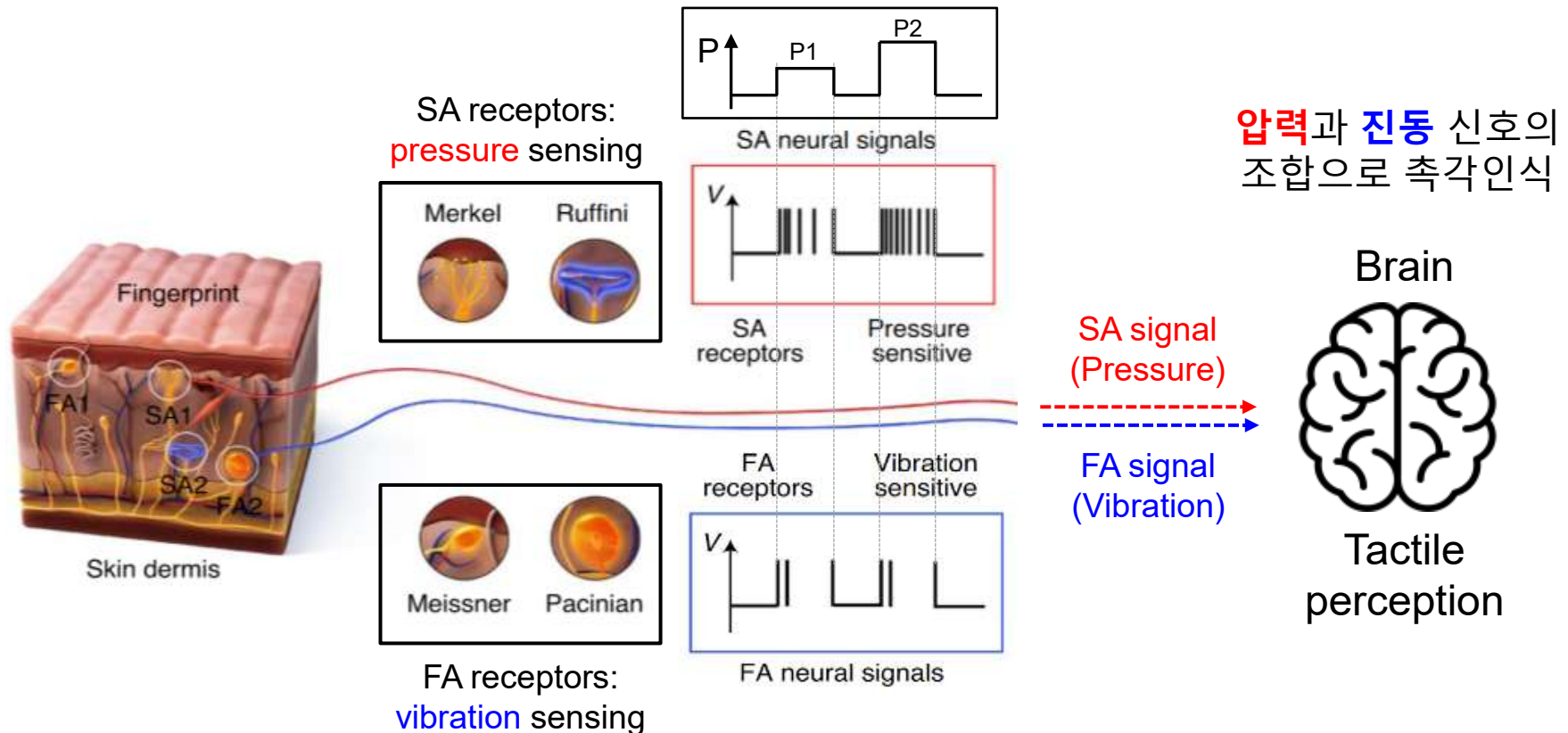
- SA receptors generate different patterns depending on the static **pressure**
- FA receptors generate spike at initial contact and final release of the stimuli (**vibration**)



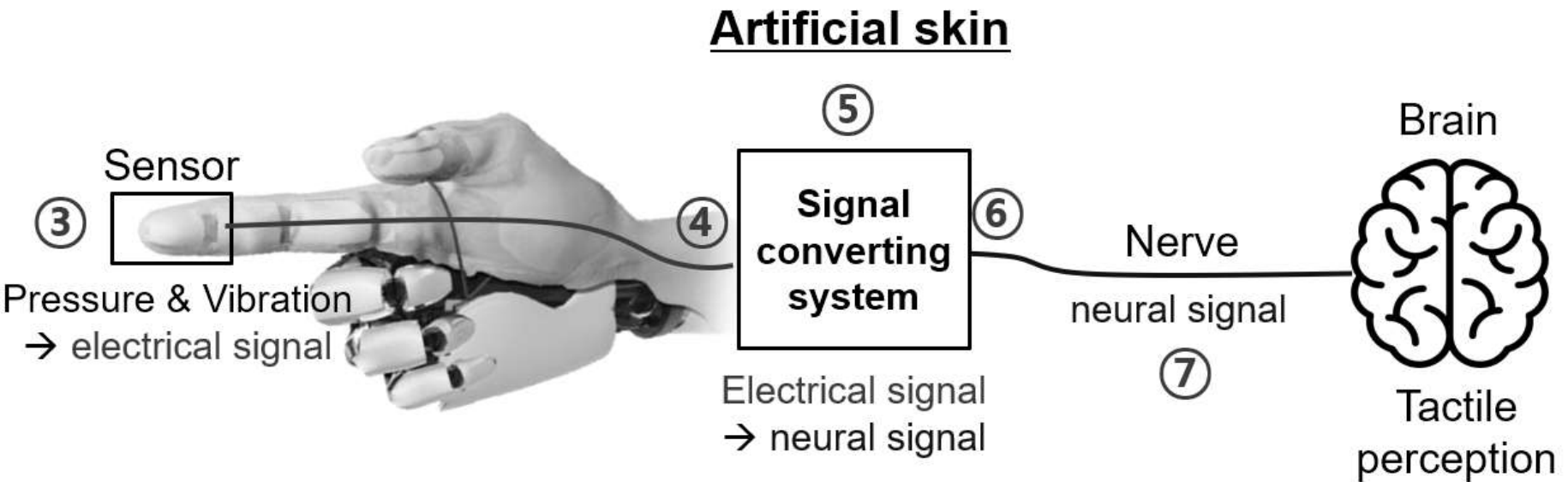
# Biological Tactile Sensory System

## ● Tactile Perception of Brain

- SA & FA signals are delivered separately, and then integrated in the human brain.
- The brain perceived tactile with a combination of the pressure and vibration signals.

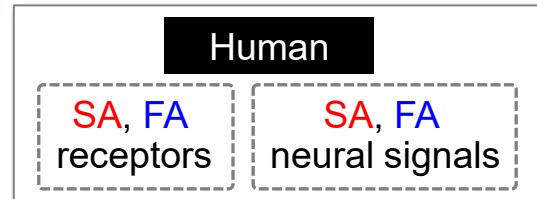
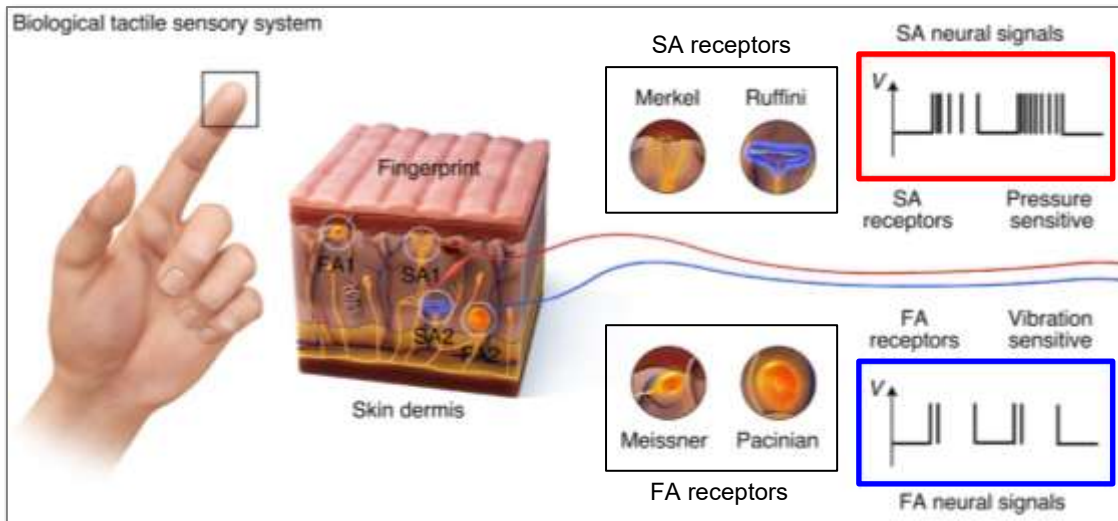


# Research Items



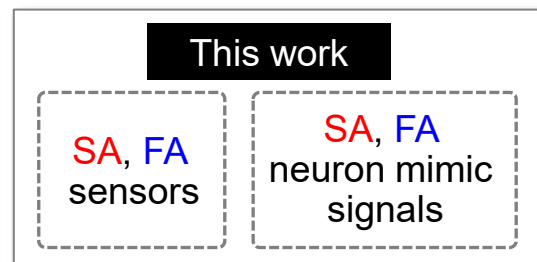
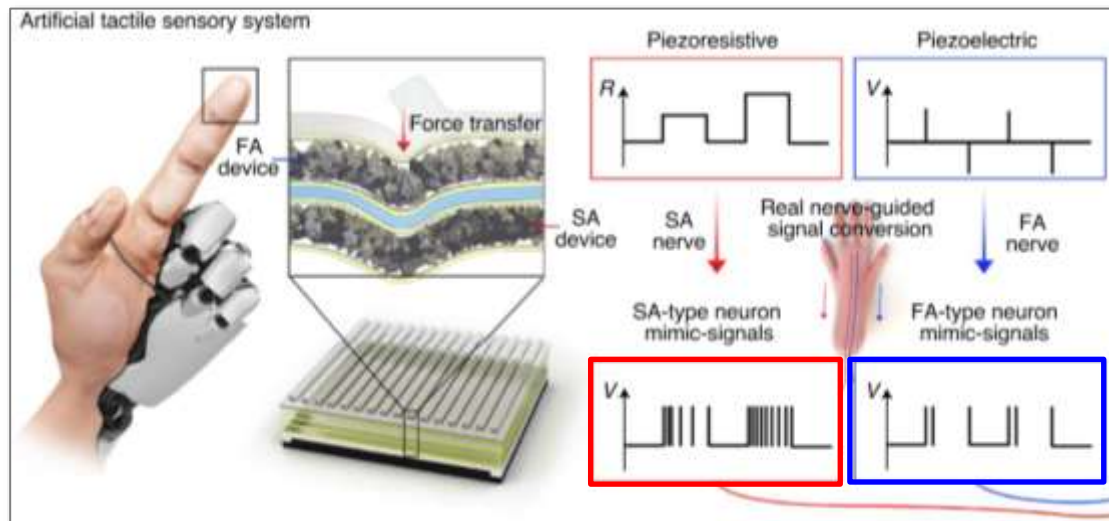
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- ⑦ **생체실험**: 신경에서 신호가 잘 전달됨을 확인하는 방법?

# Artificial Tactile Sensory System



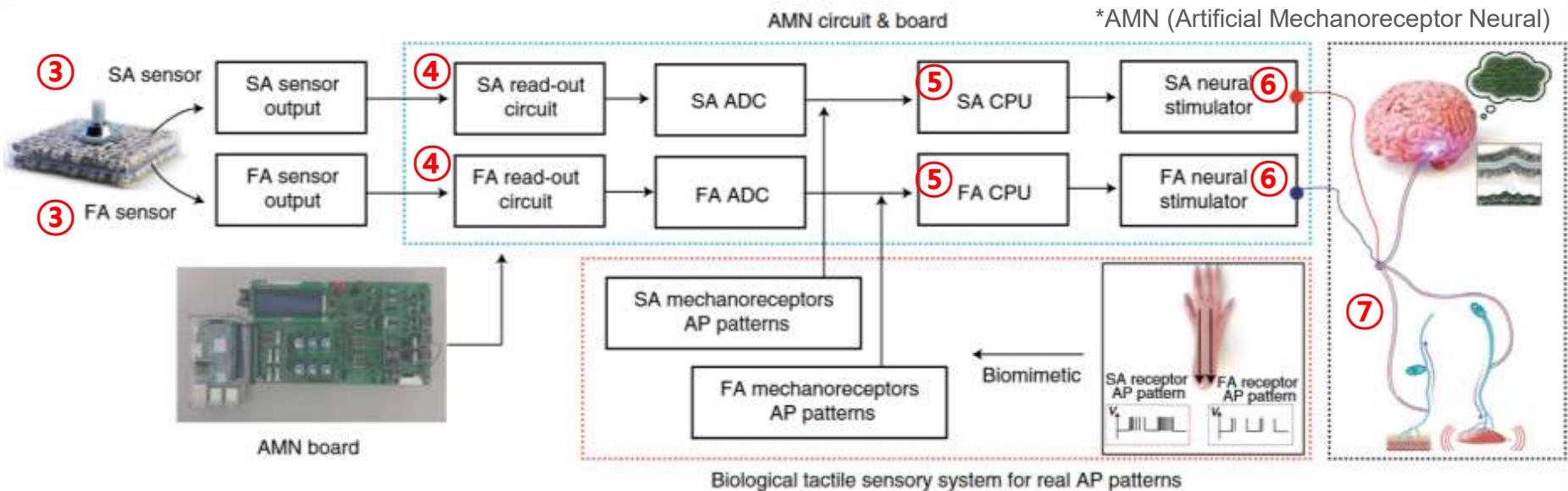
Mimicking

Mimicking

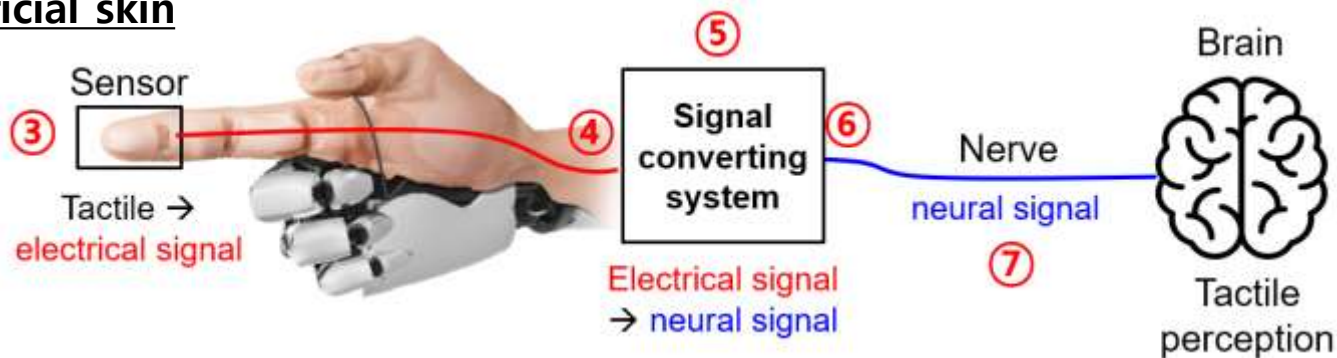


# Proposed Artificial Tactile Sensory System

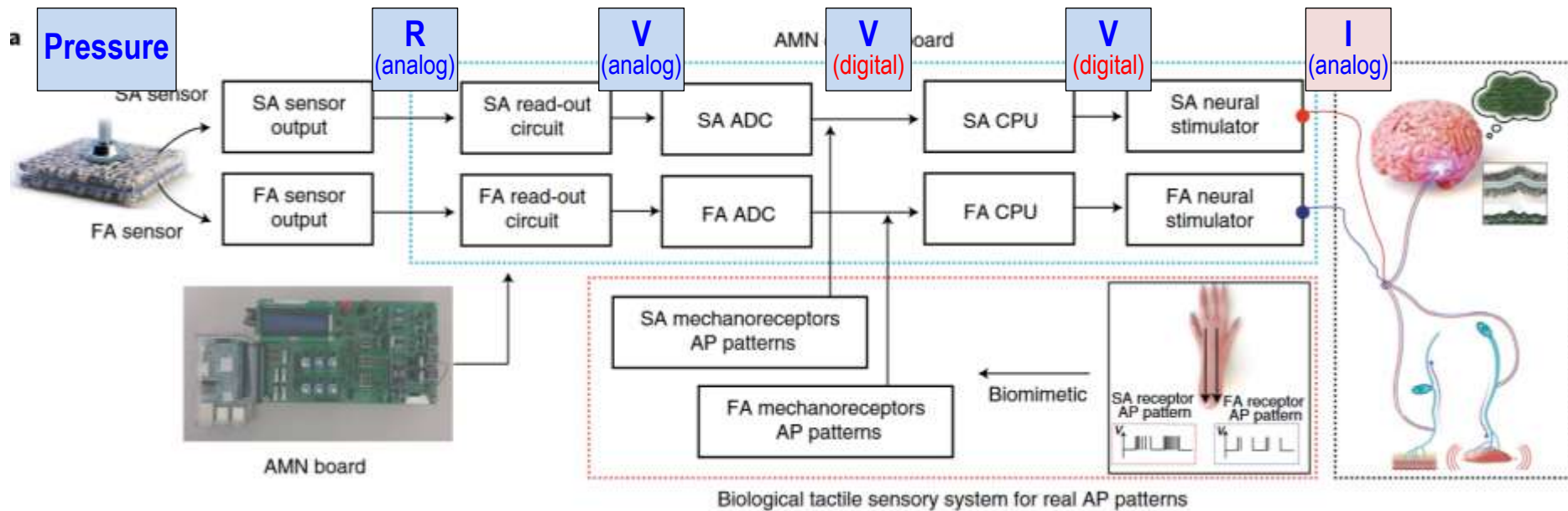
Block Diagram of the Proposed Tactile Sensory System



## Artificial skin



# Proposed Artificial Tactile Sensory System



# Novelties of The Proposed System

## ① SA & FA Sensors

- New tactile sensors with particle-based polymer composites

## ② SA & FA Mechanoreceptor's Action Potential (AP) Pattern

- SA & FA mechanoreceptor's AP patterns are obtained from real nerve of mouse

## ③ Artificial Mechanoreceptor Neural (AMN) Circuit & Board

- SA & FA sensor outputs are translated to the SA & FA mimicked neural signals

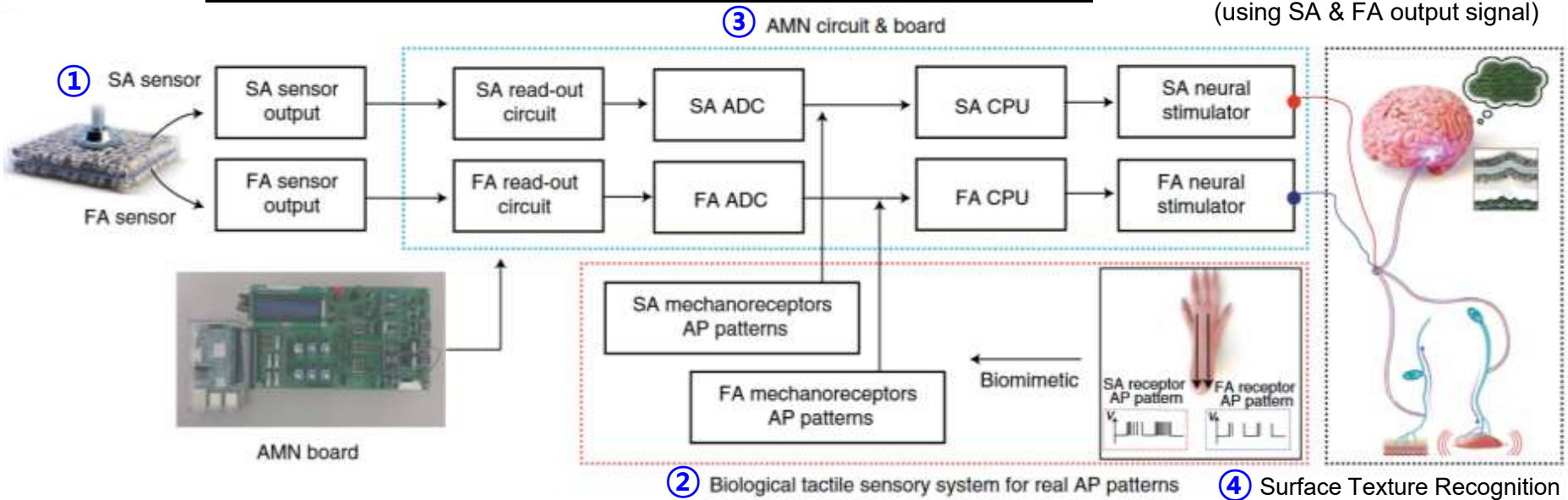
## ④ Surface Texture Recognition

- Texture recognition accuracy is verified using deep learning.

## ⑤ In vivo & Ex vivo Animal Experiments

- Neural signals generated by the proposed system are verified with in vivo & ex vivo experiments

Block Diagram of the Proposed Tactile Sensory System



# ① T-Skin Sensor

## ● T-Skin Film

- Combination of **rGO** (reduced graphene oxide) & **BaTiO<sub>3</sub>** (Barium Titanate)
- **rGO**: changes conductivity according to the magnitude of pressure  
→ **SA receptor mimicking**
- **BaTiO<sub>3</sub>** : generates piezoelectric potential according to the changes of pressure  
→ **FA receptor mimicking**

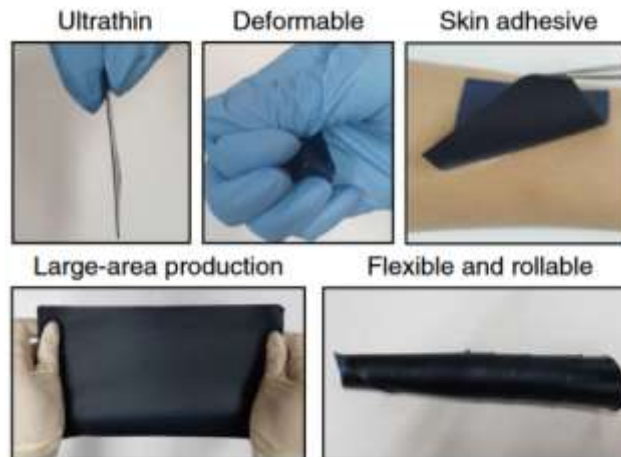
## ● T-Skin Sensor

- **rGO** enriched film → **SA sensor**
- **BaTiO<sub>3</sub>** enriched film → **FA sensor**
- Vertically stacked → **SA** and **FA** signals are generated simultaneously

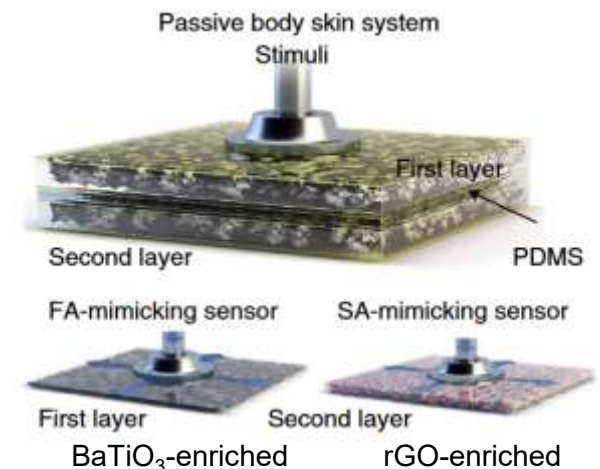
Cross-section of T-Skin Film



Characteristics of T-Skin Film



Configuration of T-Skin Sensor

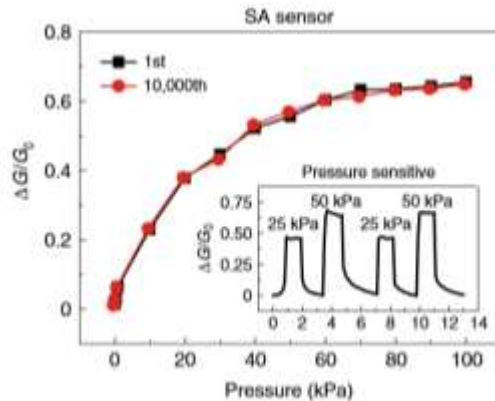


# ① T-Skin Sensor

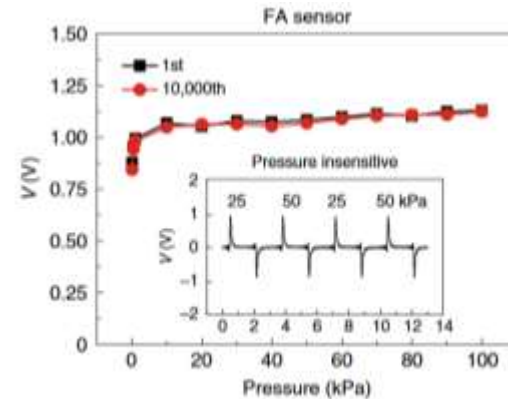
- **SA sensor** (similar to SA mechanoreceptor)
  - Pressure sensitive
- **FA sensor** (similar to FA mechanoreceptor)
  - Pressure insensitive
  - Detects high-frequency vibration (1,000Hz) \*Human vibration detection: Max. 500 Hz

Responses under static pressure (10,000 repeated measurement)

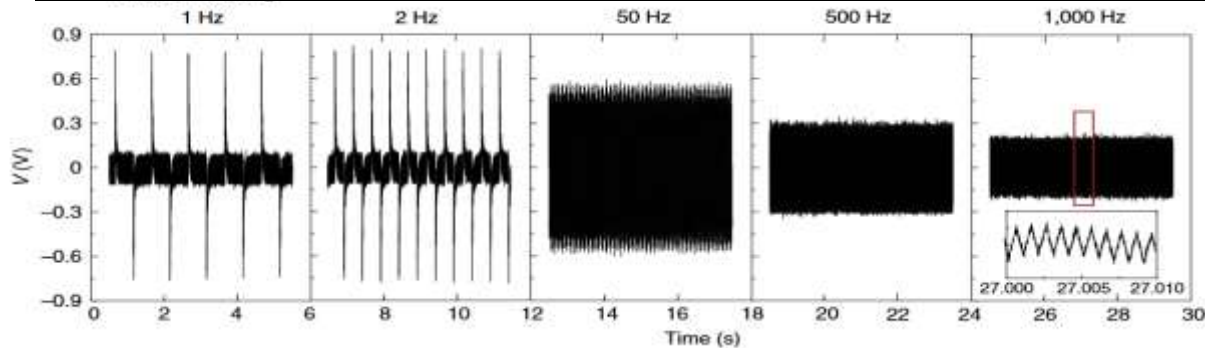
SA sensor  
(pressure sensitive)



FA sensor  
(pressure insensitive)



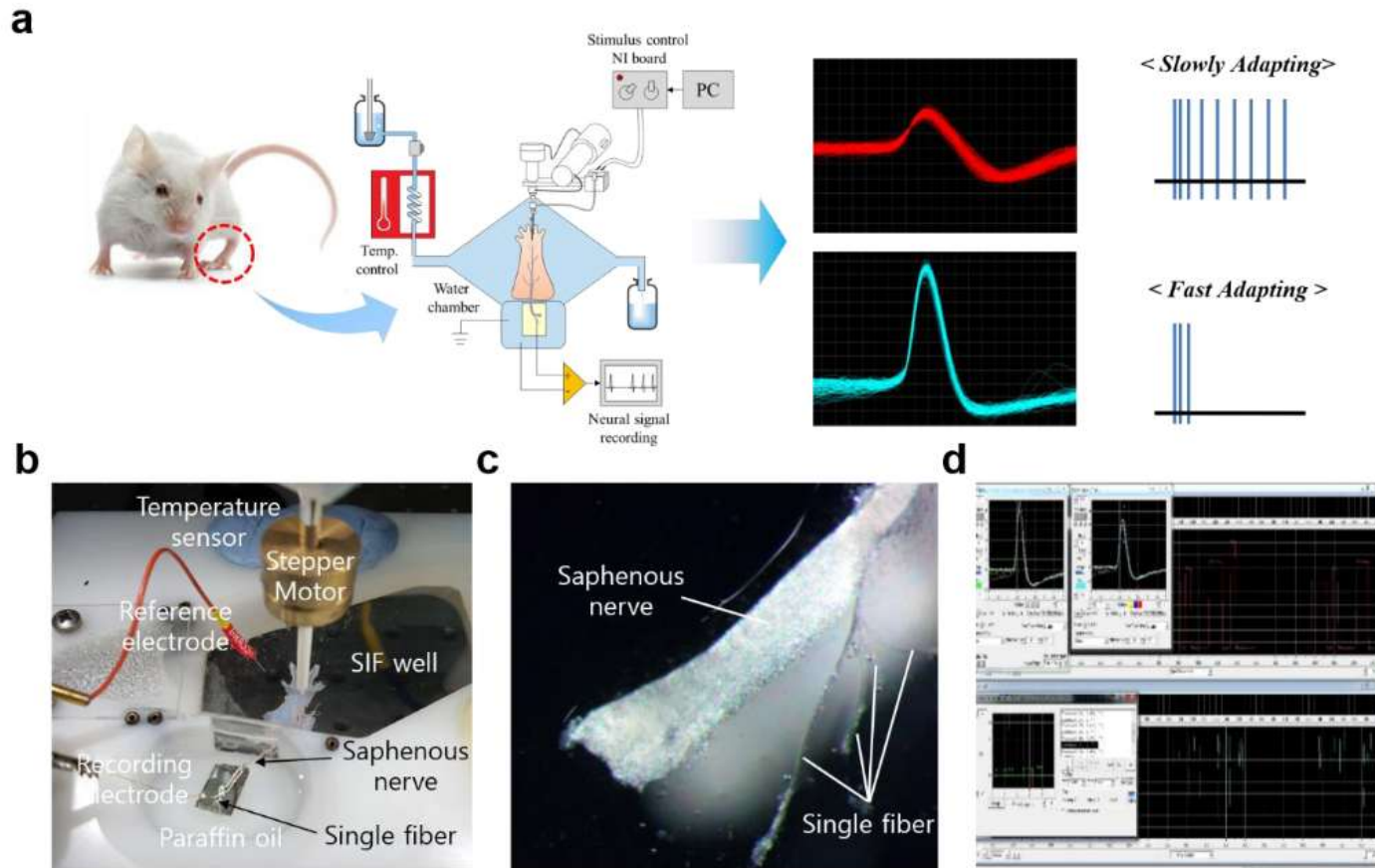
Vibration-sensing capability of the FA sensor in 1 Hz to 1,000 Hz



# ② Mechanoreceptor Action Potential (AP) Pattern

## ● Obtaining AP Pattern from Real Nerve

- AP patterns against mechanical stimuli were obtained from real nerve of mouse.
- AP patterns were collected for SA and FA mechanoreceptors independently.

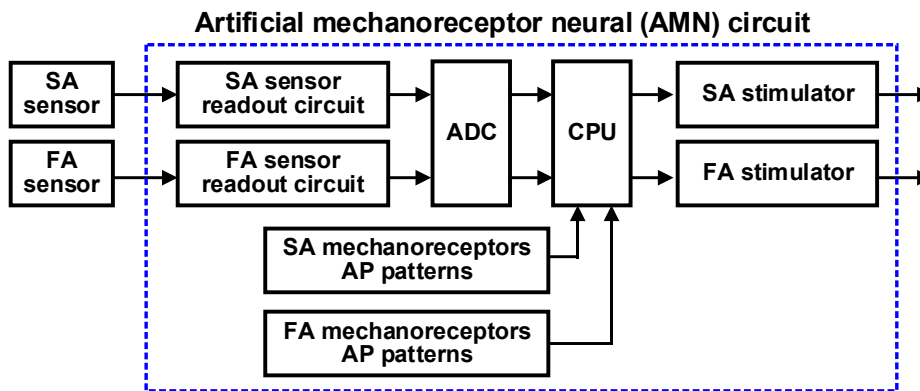


# ③ Artificial Mechanoreceptor Neural (AMN) Circuit

## ● Configuration of AMN Circuit

- Sensor readout circuit + ADC + CPU + neural stimulator
- Mechanoreceptor AP patterns are stored in nonvolatile memory.

Block Diagram of AMN Circuit



### ① Sensor Readout circuit

Converts the sensor response to voltage domain

### ② ADC

Converts voltage to digital domain

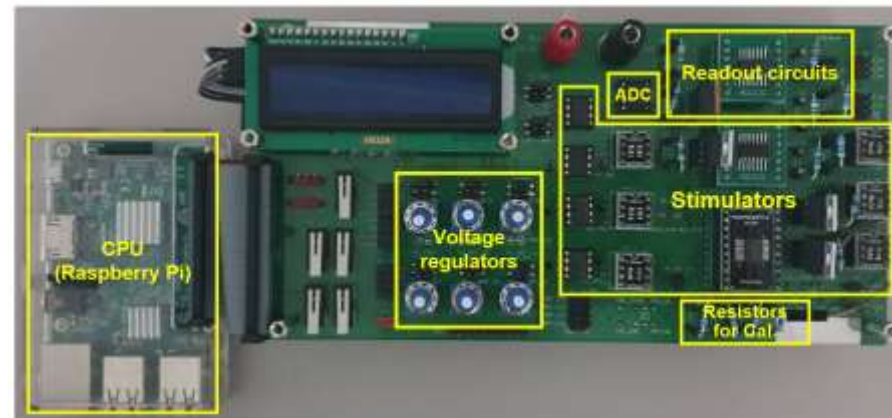
### ③ CPU (in Raspberry Pi)

Digital processing & selects AP pattern

### ④ Neural stimulator

Converts AP pattern to current domain

Fabricated AMN Circuit Board



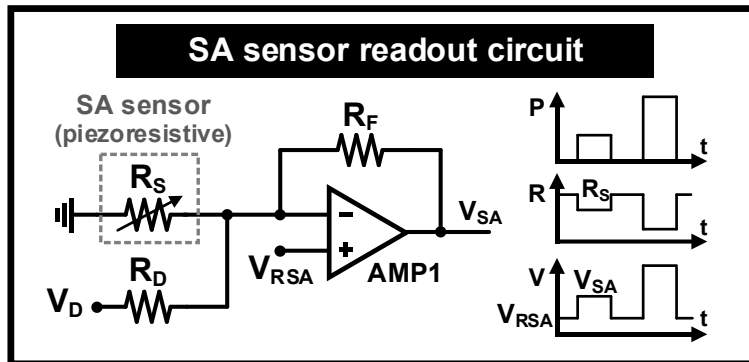
# ③ Artificial Mechanoreceptor Neural (AMN) Circuit

## ● Electrical Model of Sensor

- SA sensor: pressure dependent resistor
- FA sensor: vibration dependent current source (AC current)

## ● Sensor Readout Circuit

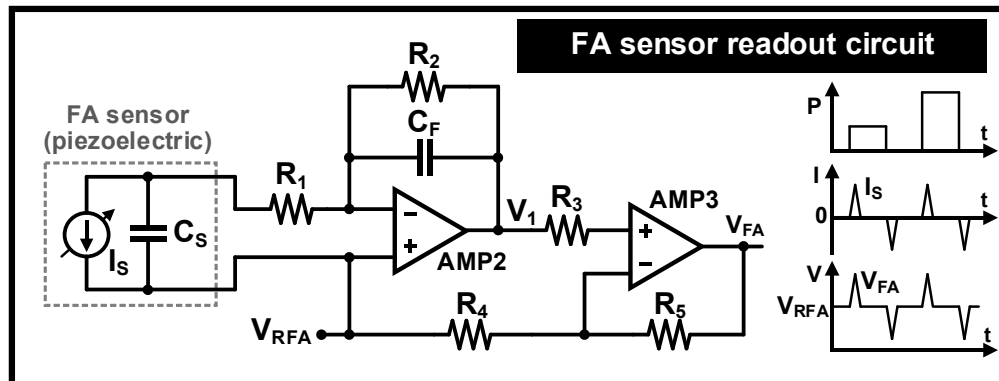
- SA readout circuit: resistance is converted to voltage level
- FA readout circuit: AC current is converted to voltage spike



Pressure on SA sensor

→ resistance (conductivity) variation

→ output voltage level change



Vibration on FA sensor

→ AC current generation

→ output voltage spike

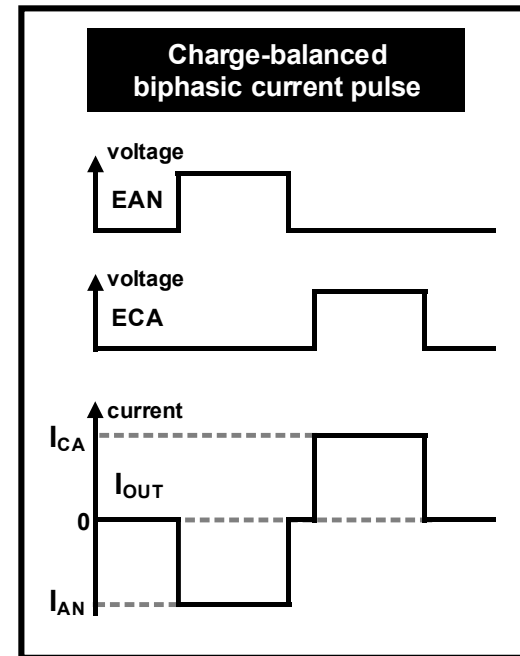
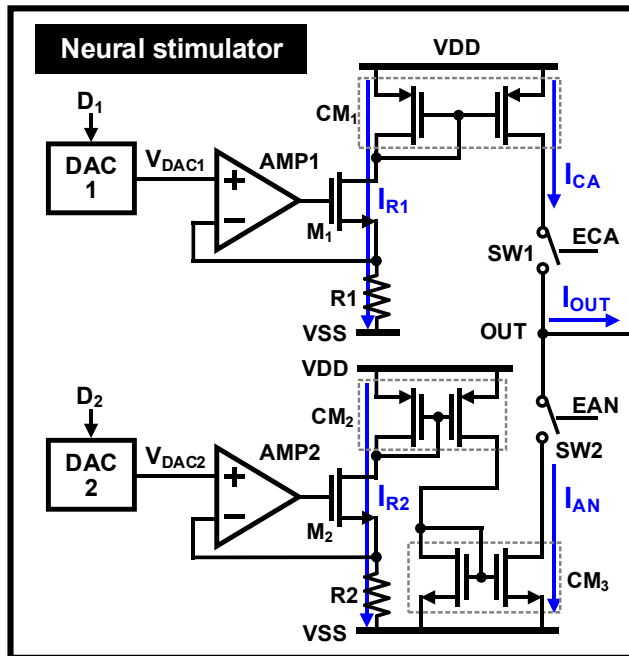
# ③ Artificial Mechanoreceptor Neural (AMN) Circuit

## ● Neural Stimulating

- “Charge balanced biphasic current pulse” method  
→ maintaining charge balance in the biological environment to prevent tissue damage

## ● Proposed Neural Stimulator

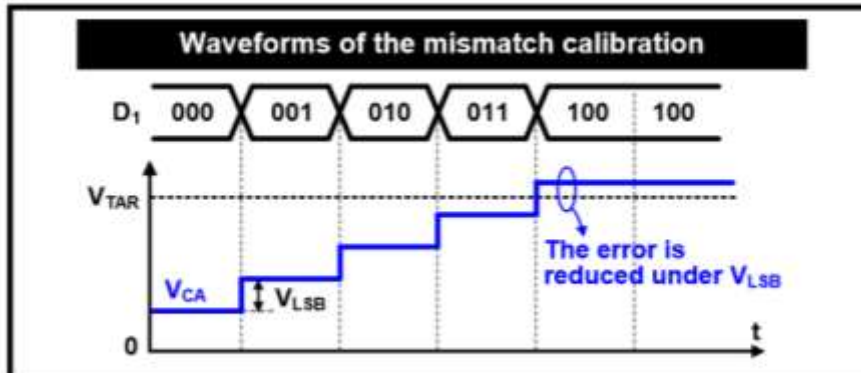
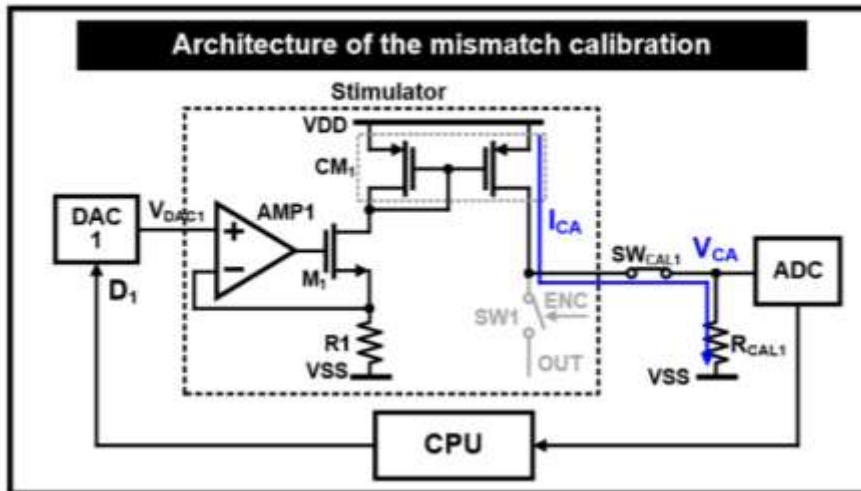
- Current mirror based current stimulator → biphasic current pulse
- Charge balance between  $I_{CA}$  &  $I_{AN}$  → prevents tissue damage during stimulation



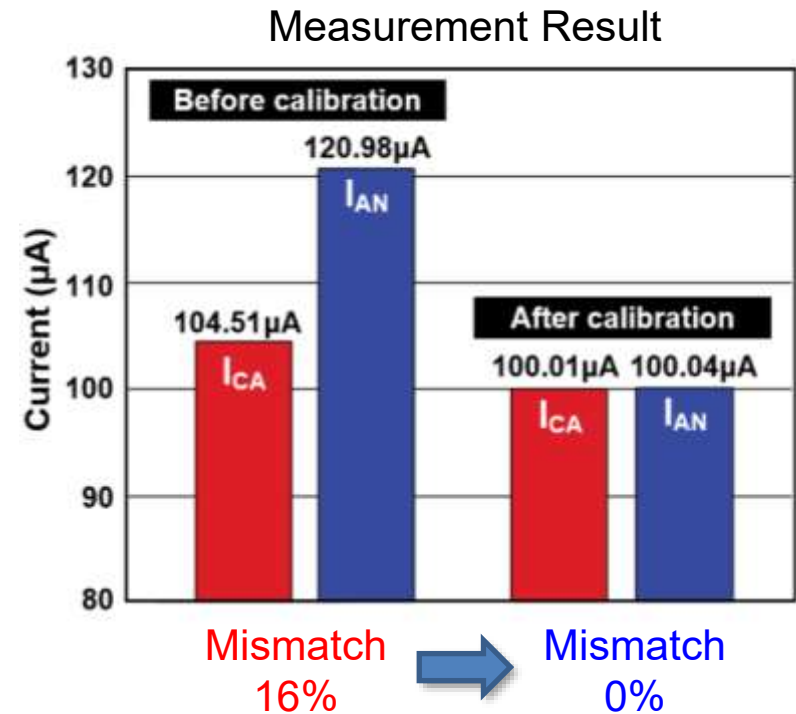
# ③ Artificial Mechanoreceptor Neural (AMN) Circuit

## ● Neural Stimulator (Calibration Method)

- Current mismatch by process variation → unbalanced charge → tissue damage
- Current mismatch calibration (by adjusting the DAC voltage) → balanced charge



\*This example uses a 3-bit DAC resolution for a simplicity.

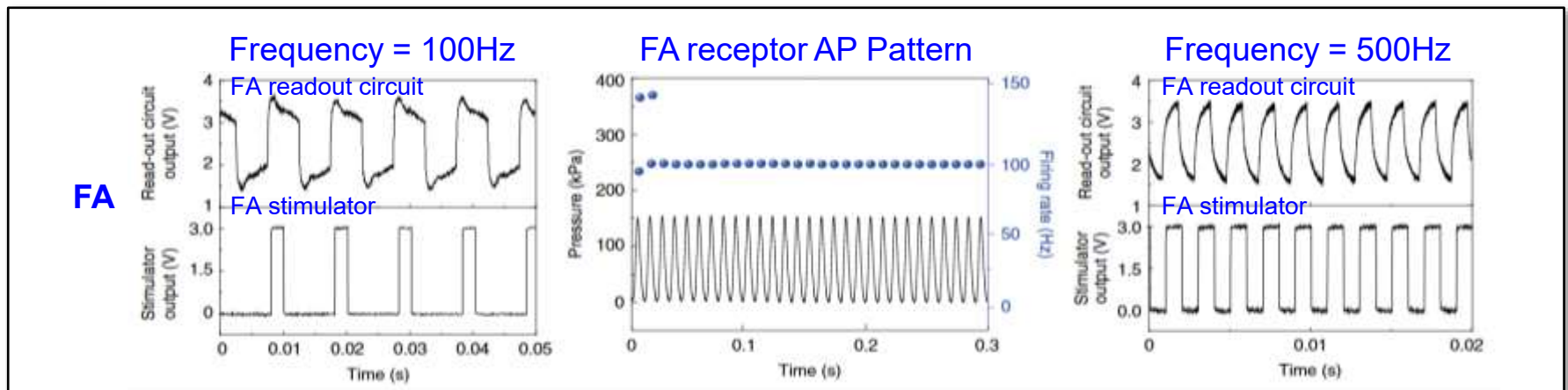
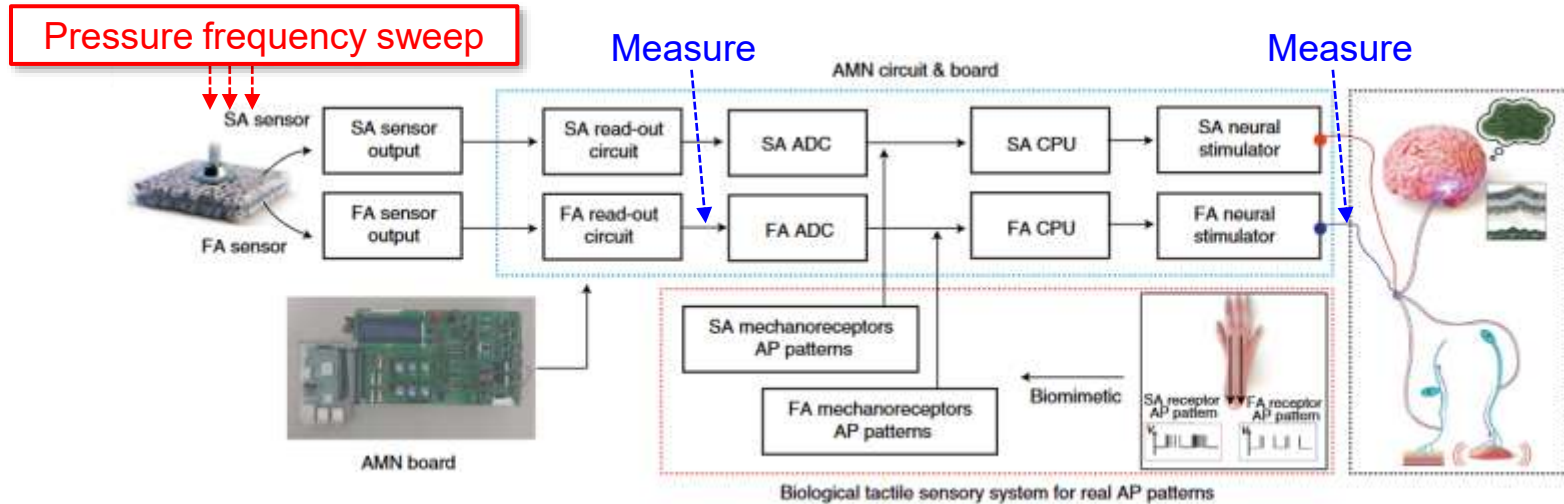




# ③ AMN Circuit - Experiments -

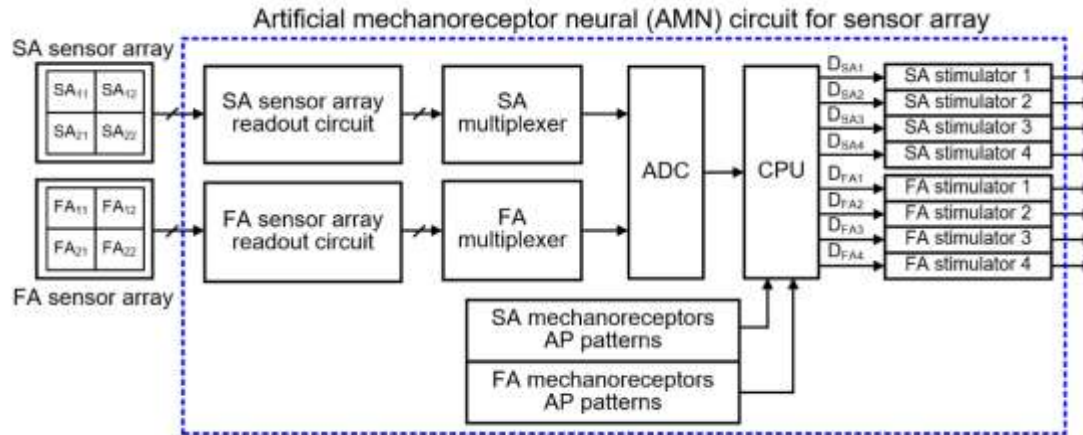
## ● Pressure Frequency Sweep

- FA circuits can cover 100Hz and 500Hz (Max 1kHz) of vibrations

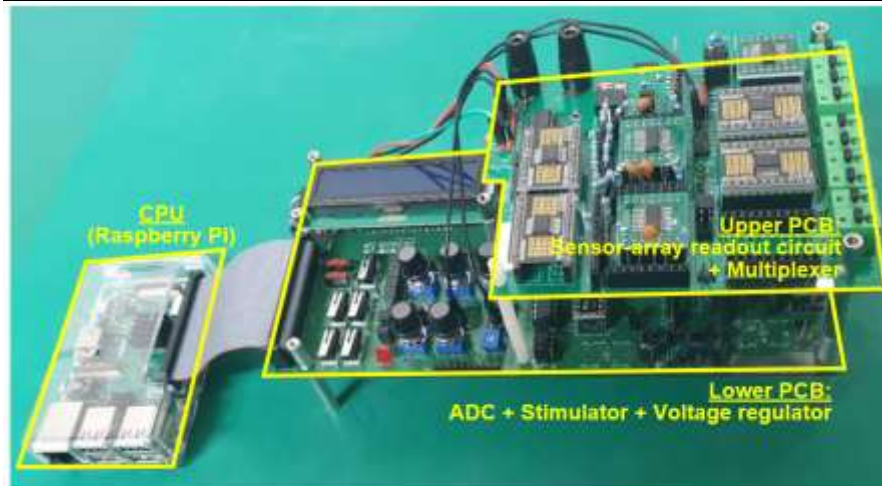


# ③ AMN Circuit - for Sensor Array -

## AMN Circuit for 2X2 Sensor Array



## AMN Circuit Board for 2X2 Sensor Array

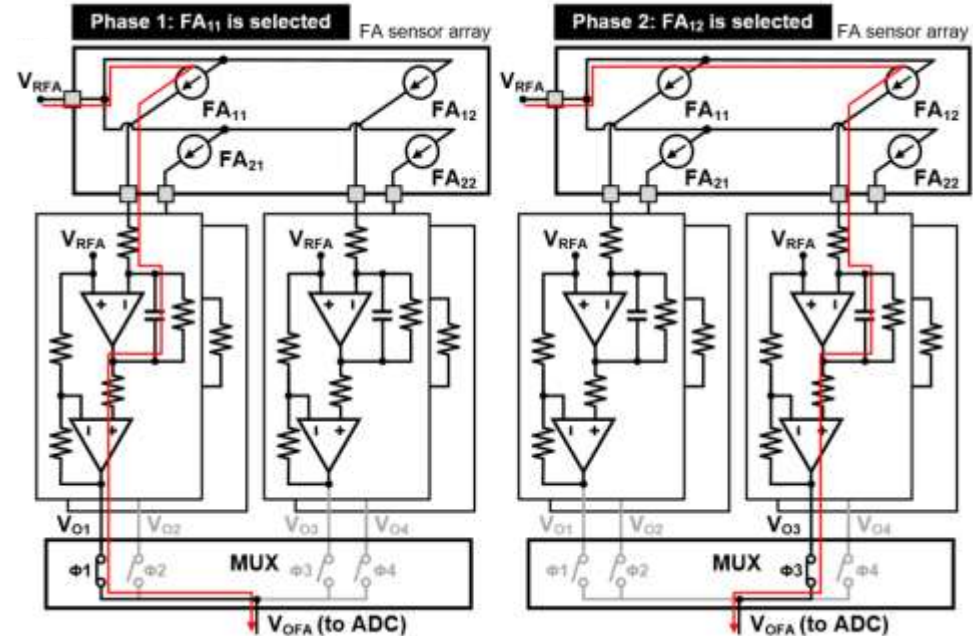
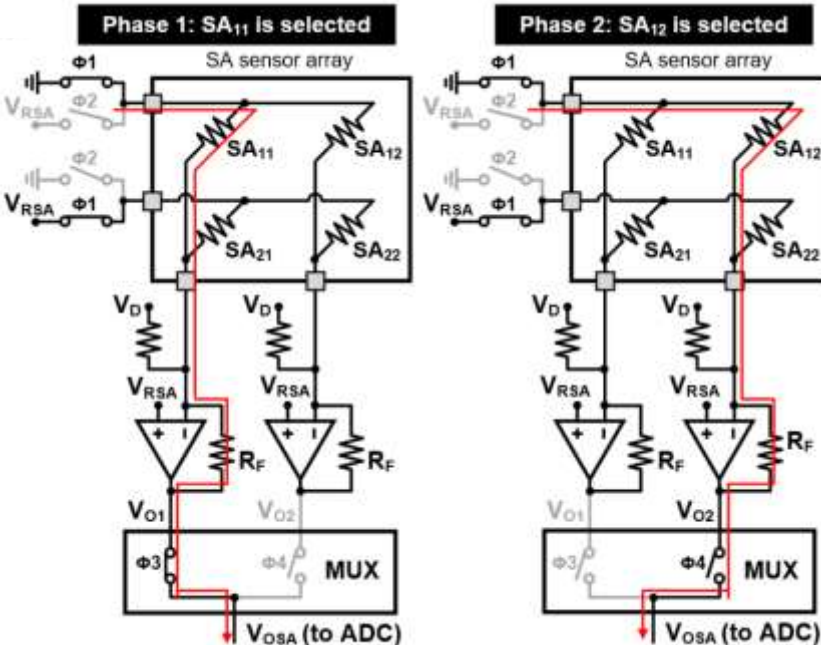


# ③ AMN Circuit - for Sensor Array -

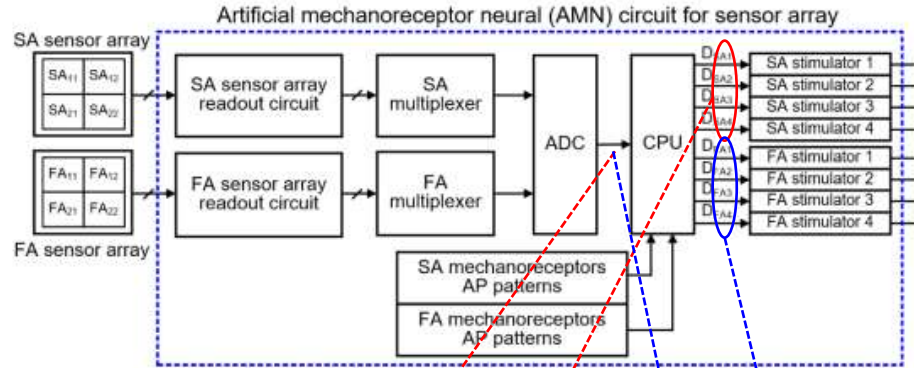
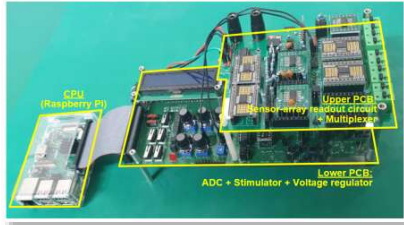
- Readout Circuits (for 2X2 Sensor Array)

SA sensor array readout circuit

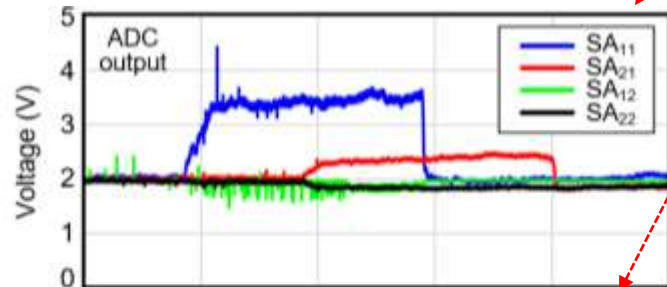
FA sensor array readout circuit



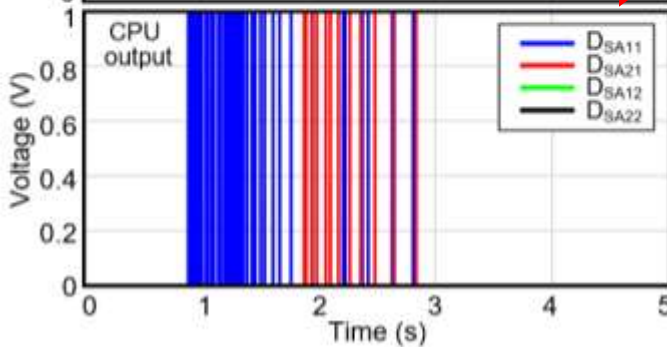
# ③ AMN Circuit - for Sensor Array -



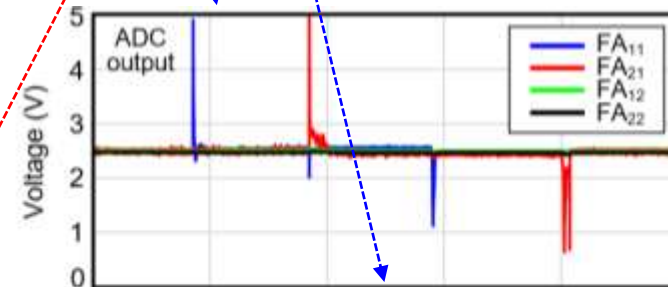
SA  
ADC



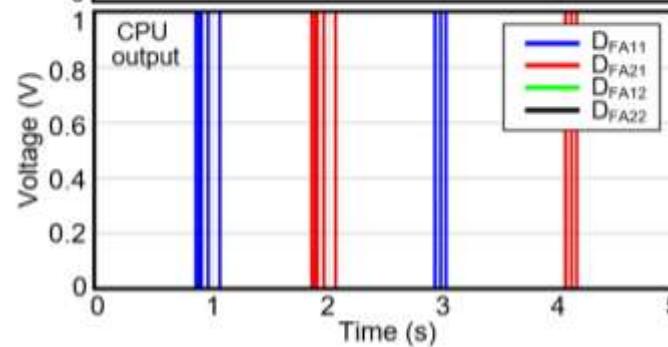
SA  
CPU



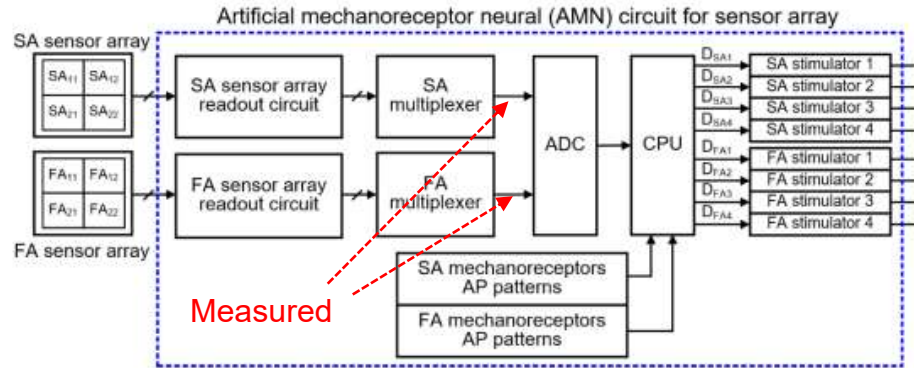
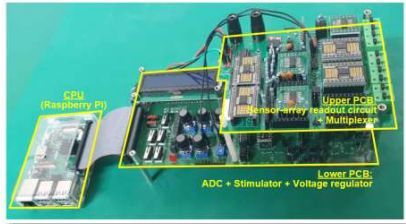
FA  
ADC



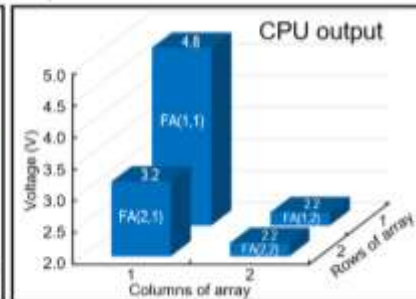
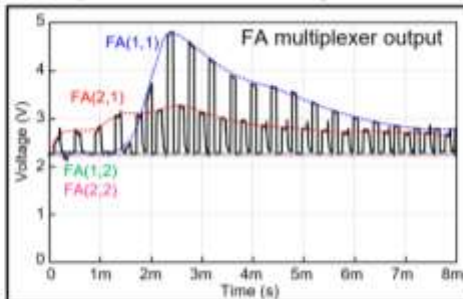
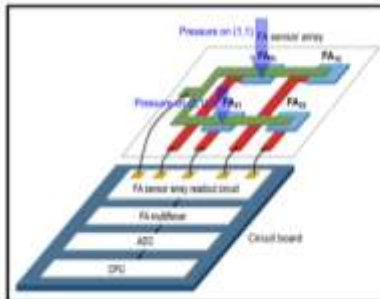
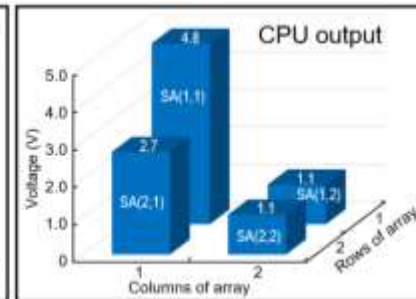
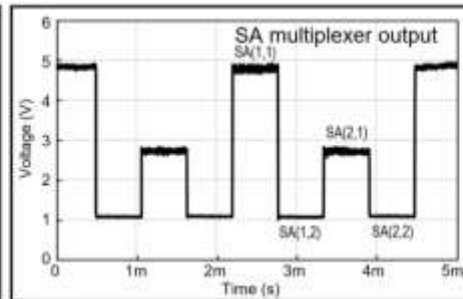
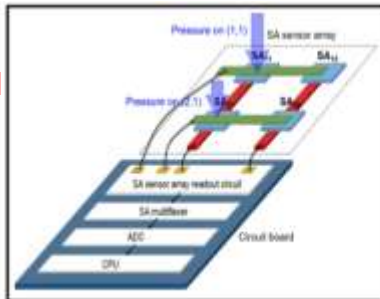
FA  
CPU



# ③ AMN Circuit - for Sensor Array -



Pressure is selectively applied to the array

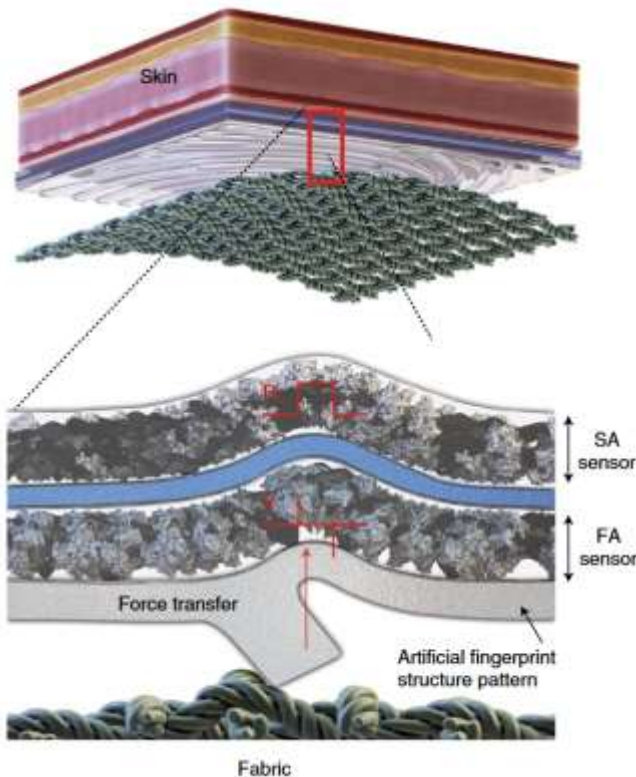


# ④ Surface Texture Recognition

## ● Proposed T-skin System

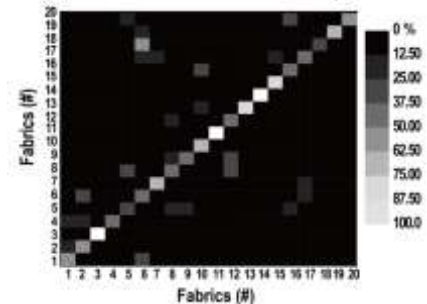
- Higher texture classification accuracy (99.1%) after combining SA and FA signals using deep learning

### Active Finger Skin System



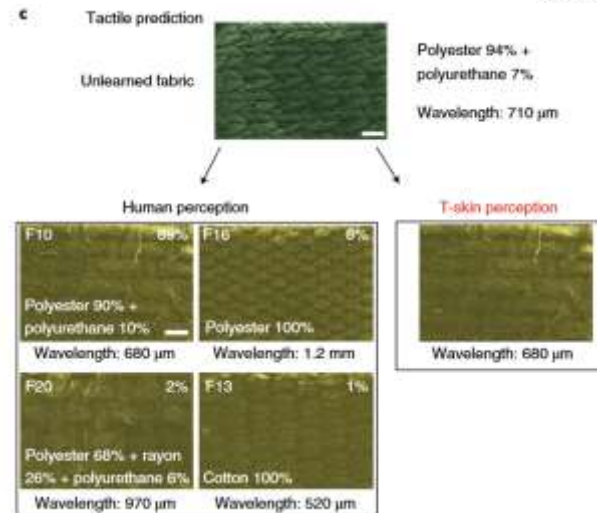
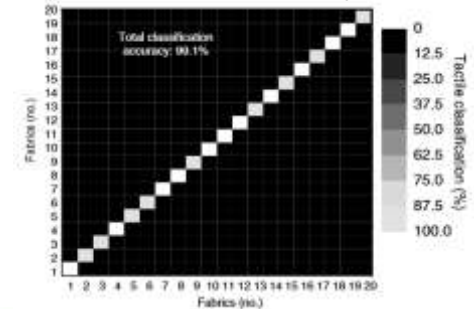
### Texture Classification (Human)

Classification accuracy: 59.1%

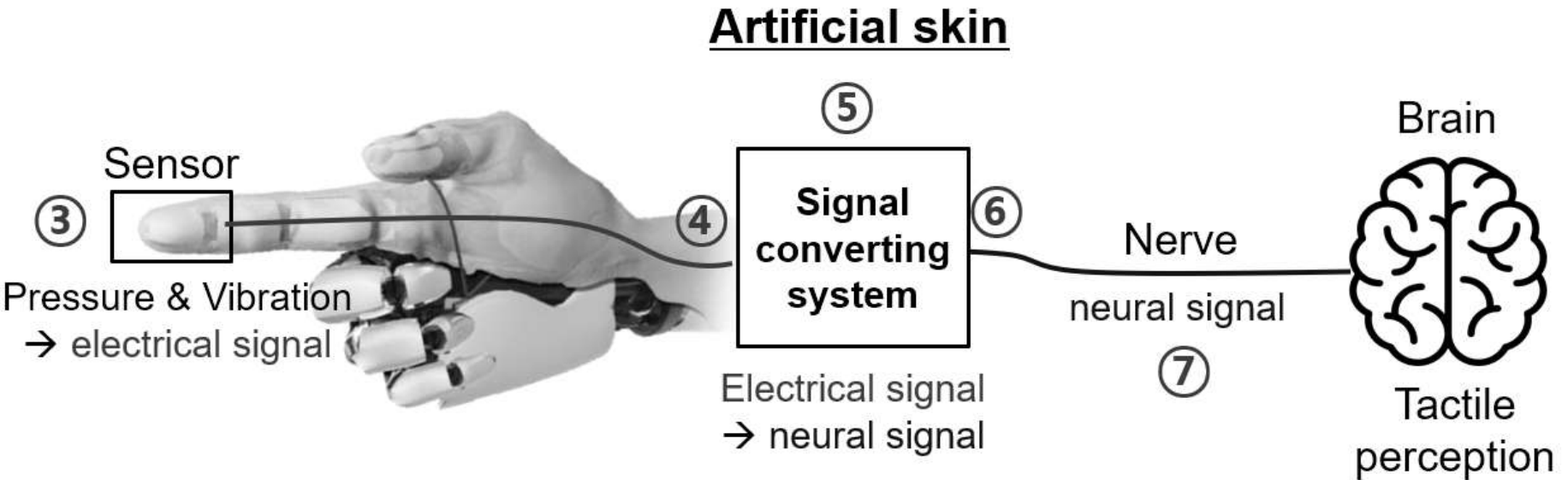


### Texture Classification (T-Skin)

Classification accuracy: 99.1%



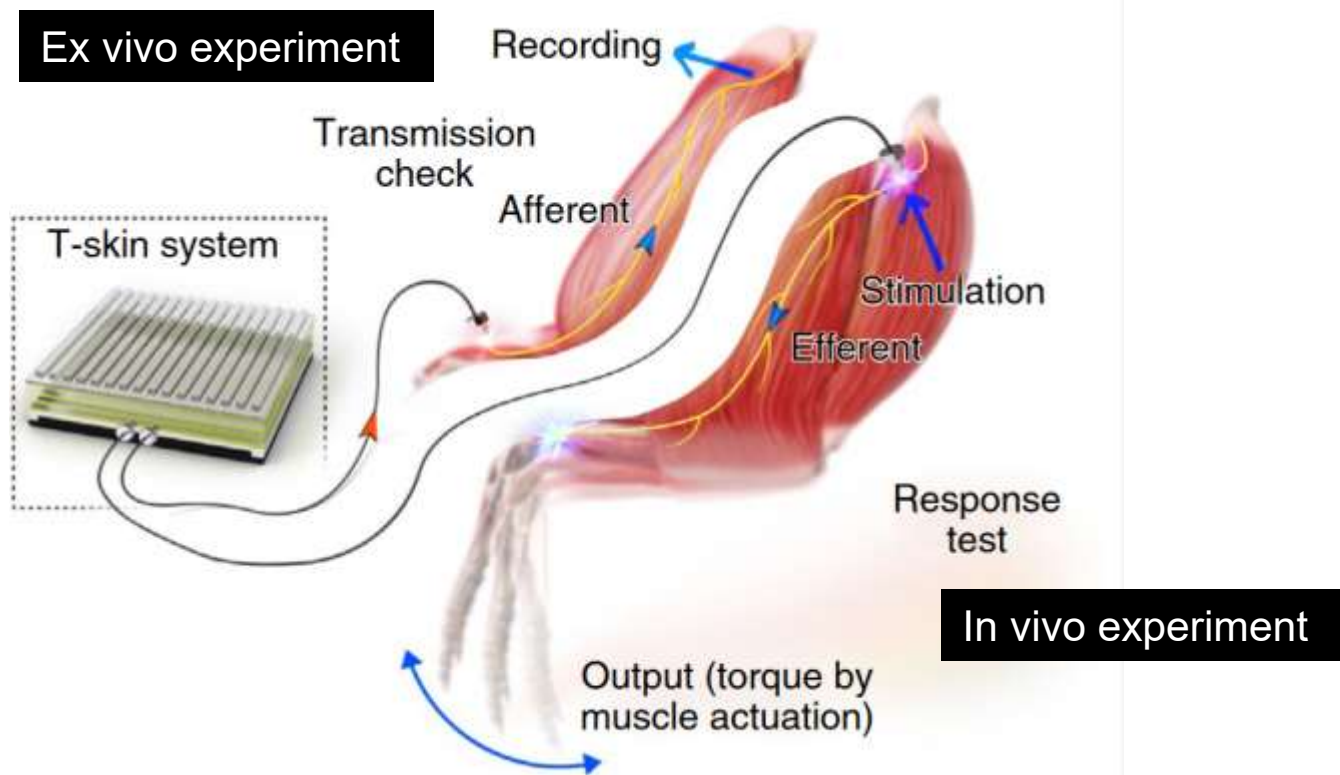
# Research Items



- ③ **센서**: 인간 촉각수용체(receptor) 를 어떻게 모방할 수 있나?
- ④ **센서 readout**: 센서 전기 신호를 왜곡 없이 읽는 방법?
- ⑤ **Signal converting**: 센서에 인가된 물리적 정보를 판단하고, neural signal을 생성
- ⑥ **Neural stimulator**: 신경이 인식할 수 있는 형태로 신호 변경 및 신경 구동
- ⑦ **생체실험**: 신경에서 신호가 잘 전달됨을 확인하는 방법?

# ⑤ Animal Experiment

- #1. **Ex vivo Experiment** (목적: 생성한 신호가 신경을 통해 전달됨을 확인)
  - To check the transmission of the generated signals in the **explanted afferent nerve**.
- #2. **In vivo Experiment** (목적: 생성한 신호로 근육 자극이 가능함을 확인.)
  - To confirm that **efferent nerve** stimulation would generate the response of the hindlimb muscle.

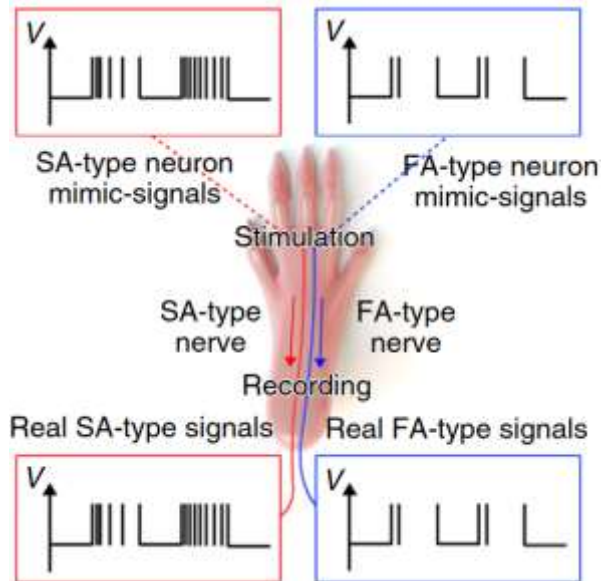


# ⑤ Animal Experiment

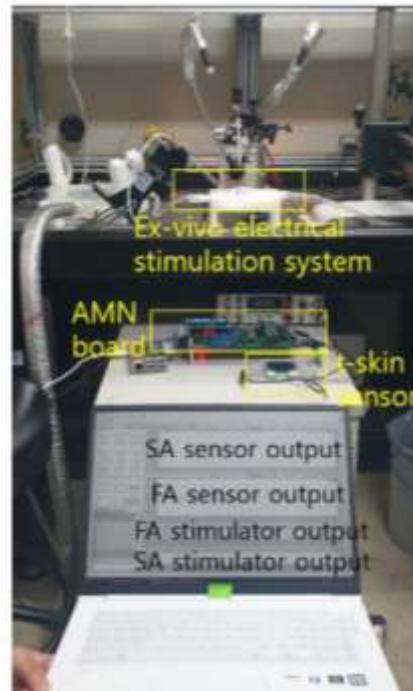
## ● #1. Ex vivo Experiment

- To check the transmission of the SA & FA signals in the explanted afferent nerve.
- SA & FA signals are applied to a single fiber in skin from hindlimb of mouse

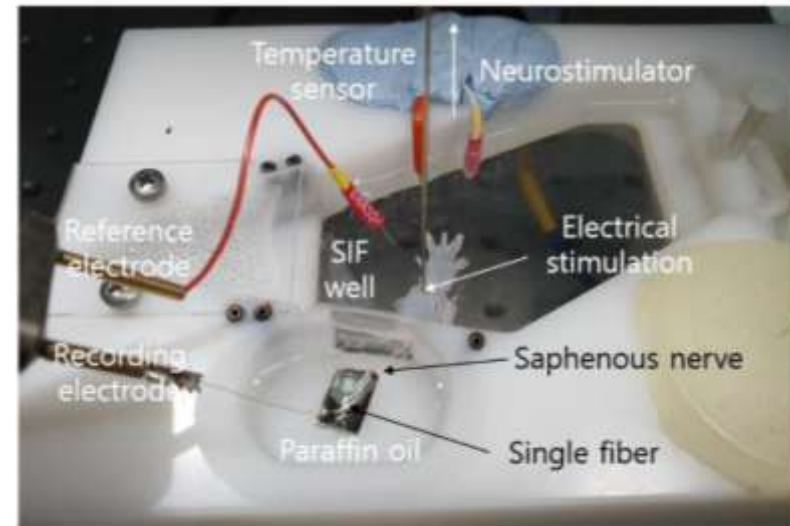
Concept



Experiment Setup



Experiment Setup

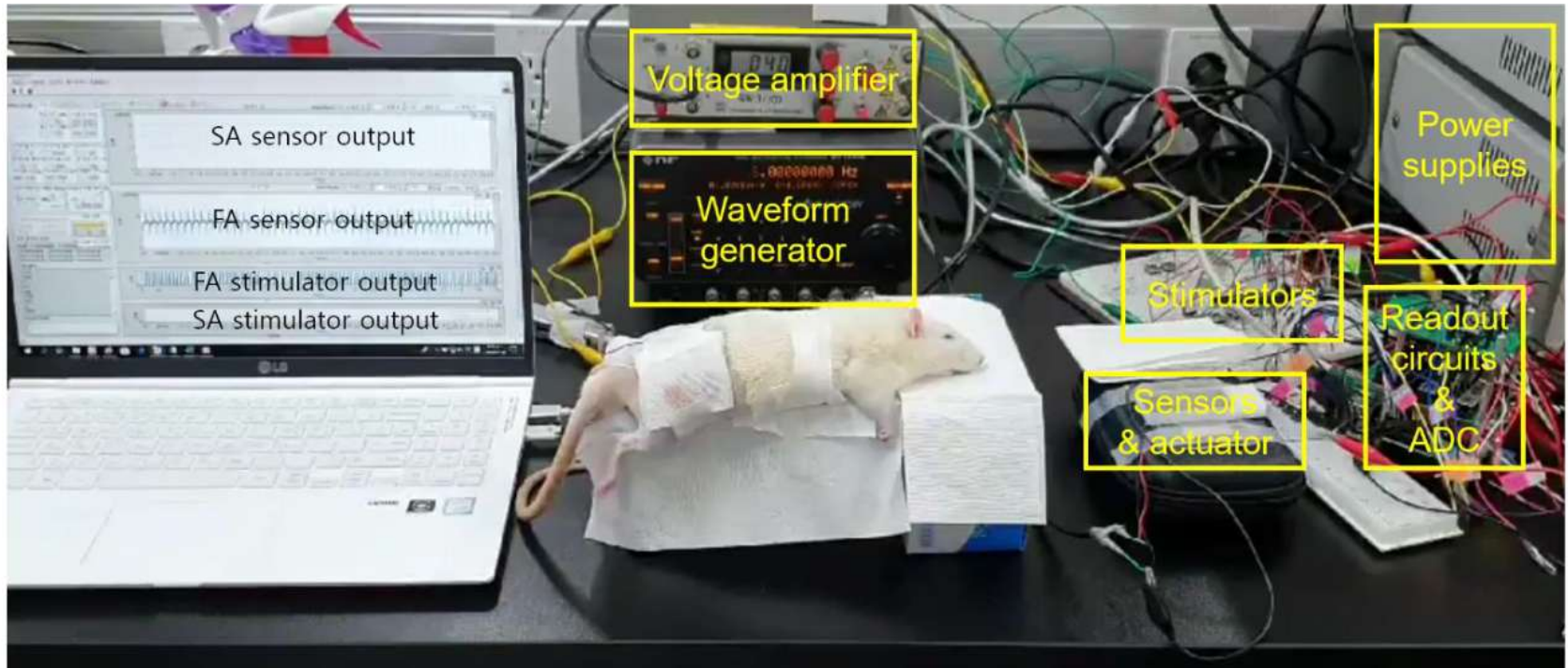


# ⑤ Animal Experiment

## ● #2. In vivo Experiment

- To confirm that **afferent nerve** stimulation would generate the response of the hindlimb muscle.

### Experiment Setup



# Human Skin Vs. Proposed T-Skin

Main skin functions		Real human skin	Proposed tactile skin
Slow adaptive	Pressure sensitivity	Sensitive to pressure	0.01/kPa (0.1-50 kPa) 0.002/kPa (50-100 kPa)
	Pressure detection range	0.1 ~ 100 kPa	0.1 ~ 100 kPa
	Stretchability	< 40-50%	< 100%
Fast adaptive	Response time	> 2 ms for Pacinian Corpuscle	> 1 ms for FA sensors
	Frequency range	< Max. 500 Hz for Pacinian Corpuscle	< 1,000 Hz for FA sensors
Skin	Durability	Infinite without pain	< 10,000 cycles
Main property	Stimuli selectivity	SA and FA receptors are selectively sensitive to pressure and vibration	SA and FA sensors are selectively sensitive to pressure and vibrations

# Research Team

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- **Researchers**

- Prof. Jong-Seok Kim (Hanyang Univ.): Co-first author
- Prof. Sungwoo Chun (Korea Univ.): Co-corresponding author, Co-first author
- Prof. Seongjun Park (KAIST): Co-corresponding author
- Yongsang Yoo (Hanyang Univ.)
- Youngin Choi (Hanyang Univ.)
- Prof. Sung Jun Jung (Hanyang Univ.)
- Prof. Dongpyo Jang (Hanyang Univ.)
- Gwangyeob Lee (Yonsei Univ.)
- Kang-Il Song (KIST)
- Kum Seok Nam (KAIST)
- Inchan Youn (KIST)
- Prof. Donghee Son (KIST, Sungkyunkwan Univ)
- Prof. Chaghyun Pang (Sungkyunkwan Univ)
- Yong Jeong (KAIST)
- Hachel Jung (Osong Medical Innovation Foundation)
- Young-Jin Kim (Osong Medical Innovation Foundation)
- Prof. Byong-Deok Choi (Hanyang Univ.)
- Jaehun Kim (UNIST)
- Prof. Sung-Phil Kim (UNIST)
- Prof. Wanjun Park (Hanyang Univ.)

# Research Team

언론 보도: MBC, KBS, 연합뉴스, 헤럴드경제 등



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